

ZZZ1

PCB
15'DAZ@

ZZZ2

LA-7012P
15'DA@

ZZZ3

LS-7012P
15'DA@

ZZZ4

LS-7013P
15'DA@

ZZZ5

LS-7014P
15'DA@

Compal Confidential

Schematics Document

PAW20

Montevina

with Intel Cantiga + ICH9 core logic

REV:1.0A

2010-12-24

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Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	Cover Sheet
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Clock Generator
SLG8SP556VTR

page16

Mobile Penryn

uPGA-478 CPU

page4, 5, 6

For 14"
LS-7011P 4PIN PWR/B
LS7013P Audio/B
LS7014P Touch/B

For 15"
LS-7012P 8PIN PWR/B
LS7013P Audio/B
LS7014P Touch/B

H_A#(3..35)
H_D#(0..63)



FSB
667/800MHz

CRT Connector

page21

LVDS
Connector

page22

Intel Cantiga GMCH

GM45

uFCBGA 1329

page 7, 8, 9, 10, 11, 12, 13



Dual Channel
DDR3-667/800(1.5V)

DDR3-SO-DIMM X2

BANK 0, 1, 2, 3

page 14,15

up to 4G

DMI *4



C-Link

2Channel Speaker
page26

Analog MIC_Int
page26

**Wire Less Mini
card Slot 1**

page23

6*PCL-E BUS

Intel ICH9-M

page 17,18,19,20

**SPI ROM
BIOS**

LPC BUS

EC

ENE KB926 E0

page27

AR8151/8152

10/100/Giga LAN

page24

RJ45 CONN

page25

AZALIA

Audio Codec
CONEXTAN

CX20671

page26

14*USB2.0

CMOS Camera

page22

BlueTooth CONN

page30

USB CONN X1(Right)

page29

USB PORT X1(Left)

page29

USB PORT X1(Left)

page29

Audio Jack SB CONN
HP X 1+

MIC_Ext X1

page30

Card Reader RTS5139

LPC BUS

EC

ENE KB926 E0

page27

Int.KBD

page32

**SPI ROM
BIOS**

page28

Touch Pad

page32

SATA HDD CONN

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SATA ODD CONN

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Title		Compal Electronics, Inc.	
		MB Block Diagram	
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DDR3 Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS Control Table

	SOURCE	BATT	KB926	SODIMM	CLK CHIP	WLAN WWAN	ICH9	Thermal
EC_SMB_CK1 EC_SMB_DA1	KB926 +3VALW	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926 +3VALW	X	X	X	X	X	X	V +3VS
ICH_SMBCLK ICH_SMBDATA	ICH +3VALW	X	X	V +3VS	V +3VS	V +3VALW	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM	A0	10100000
DDR SO-DIMM	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

@ FUNCTION

Structure	Description	NON-USE
45@	45 BOM	
BT@	Blue Tooth function	
CMOS@	CMOS CAMERA function	

PCIE PORT LIST

PORT	DEVICE
1	LAN
2	
3	WLAN
4	
5	
6	
7	
8	

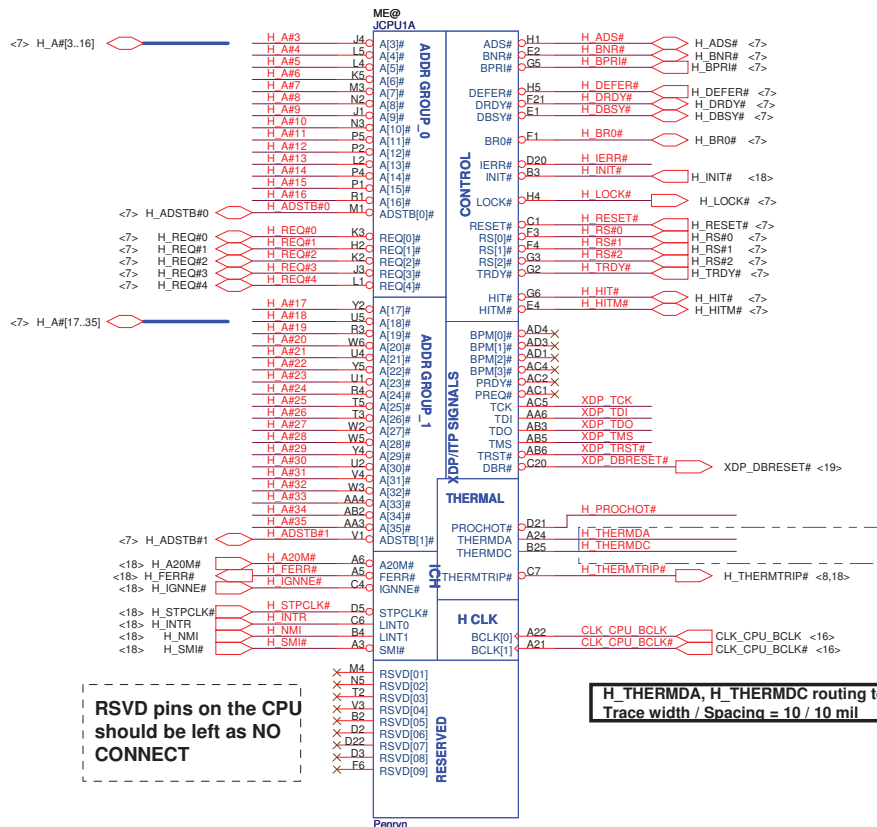
USB PORT LIST

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	
4	CARD READER
5	WIRELESS
6	BT
7	USB PORT (ESATA)
8	
9	
10	
11	
12	
13	

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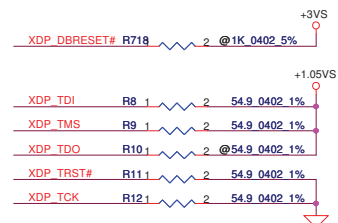
MB Notes List

LA7012P

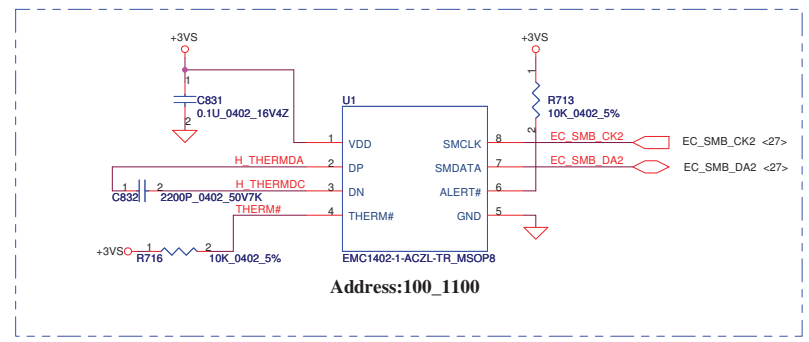
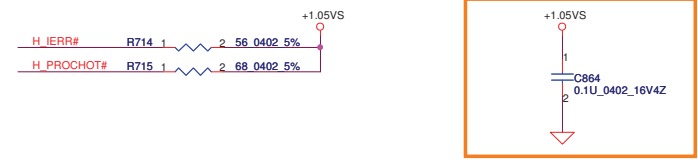


**H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil**

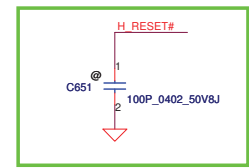
XDP Reserve for debug , Please close to CPU side



**PVT ESD solution.
Please close to R715**

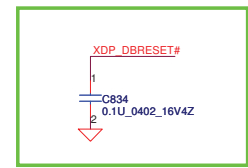


10/01 Add for reduce noise



Place closely pin C1

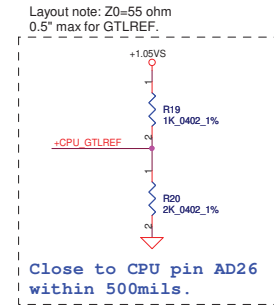
09/16 Add C834 For ESD



Place closely pin C20

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FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

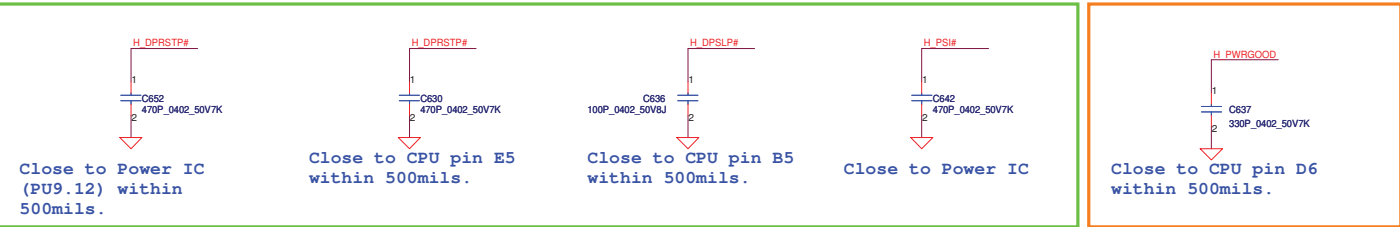


TRACE CLOSELY CPU < 0.5"

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 5mils and Space 25mils (55Ohms)

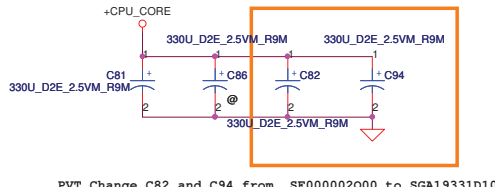
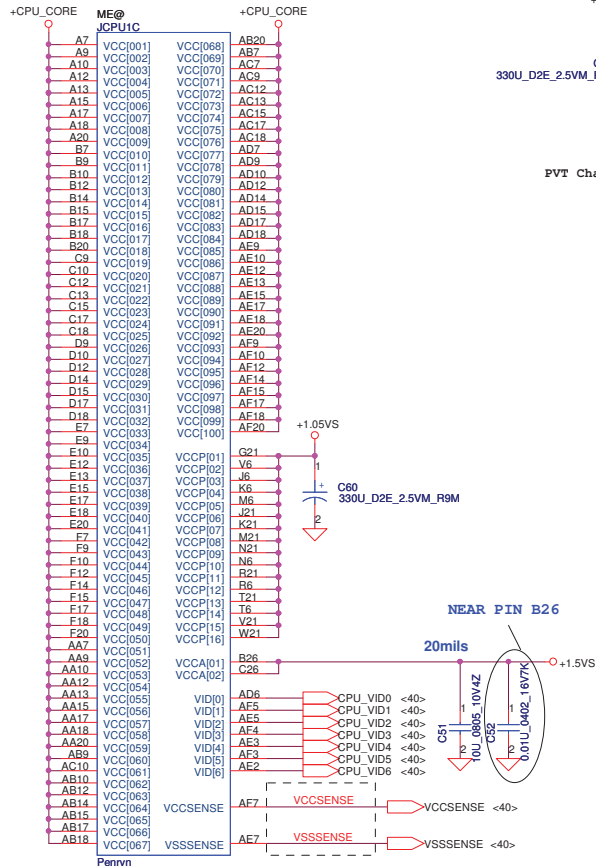
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

09/29 Add for power noise

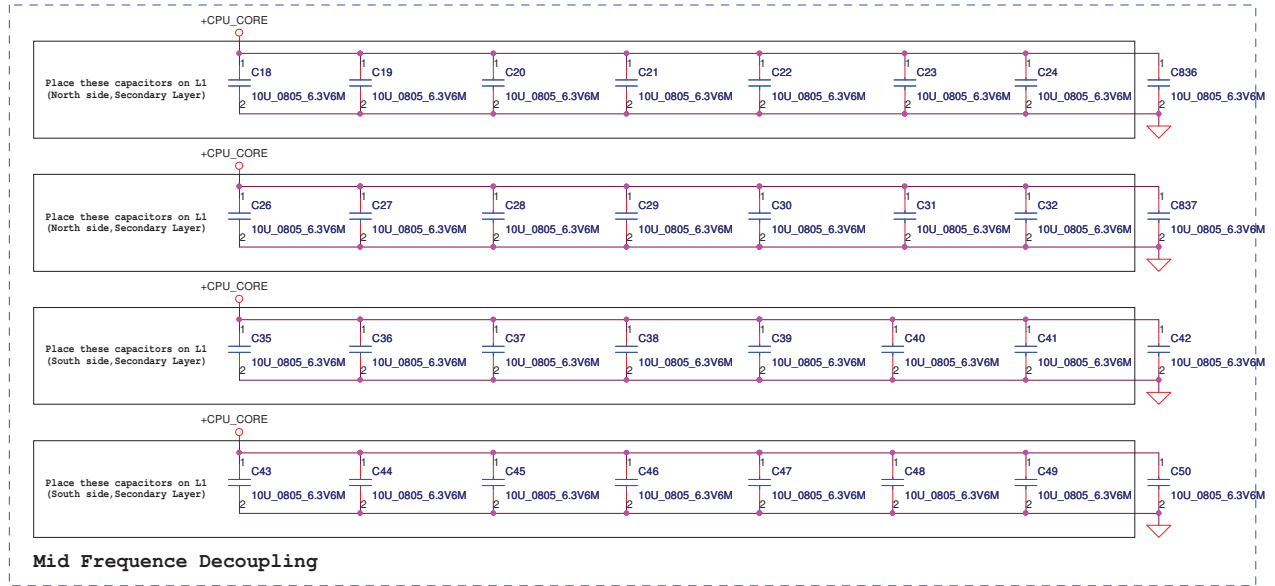
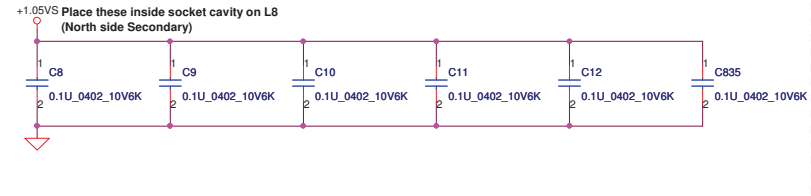


PVT for ESD solution

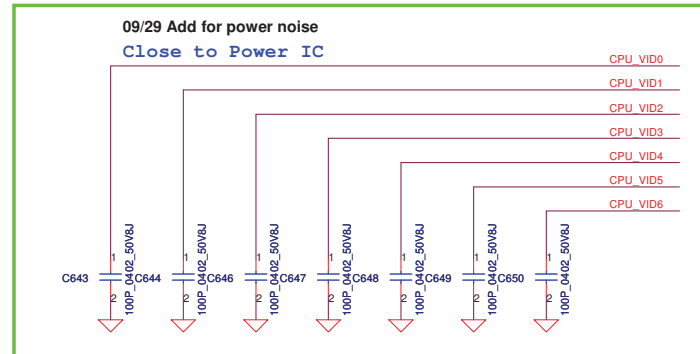
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PVT Change C82 and C94 from SF000002000 to SGA19331D10



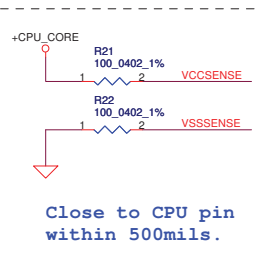
Mid Frequency Decoupling



09/29 Add for power noise
Close to Power IC

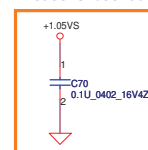
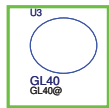
The trace width/space/other is 18/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at
27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.



Close to CPU pin
within 500mils.

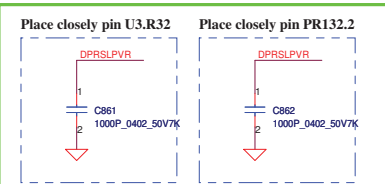
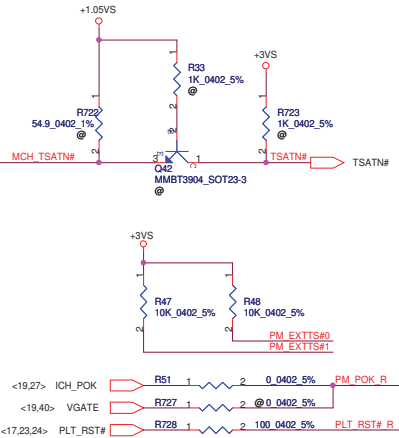
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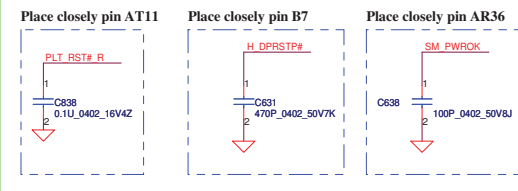
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Strap Pin Table

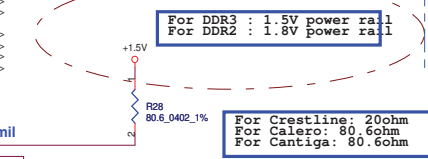
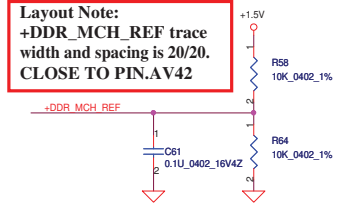
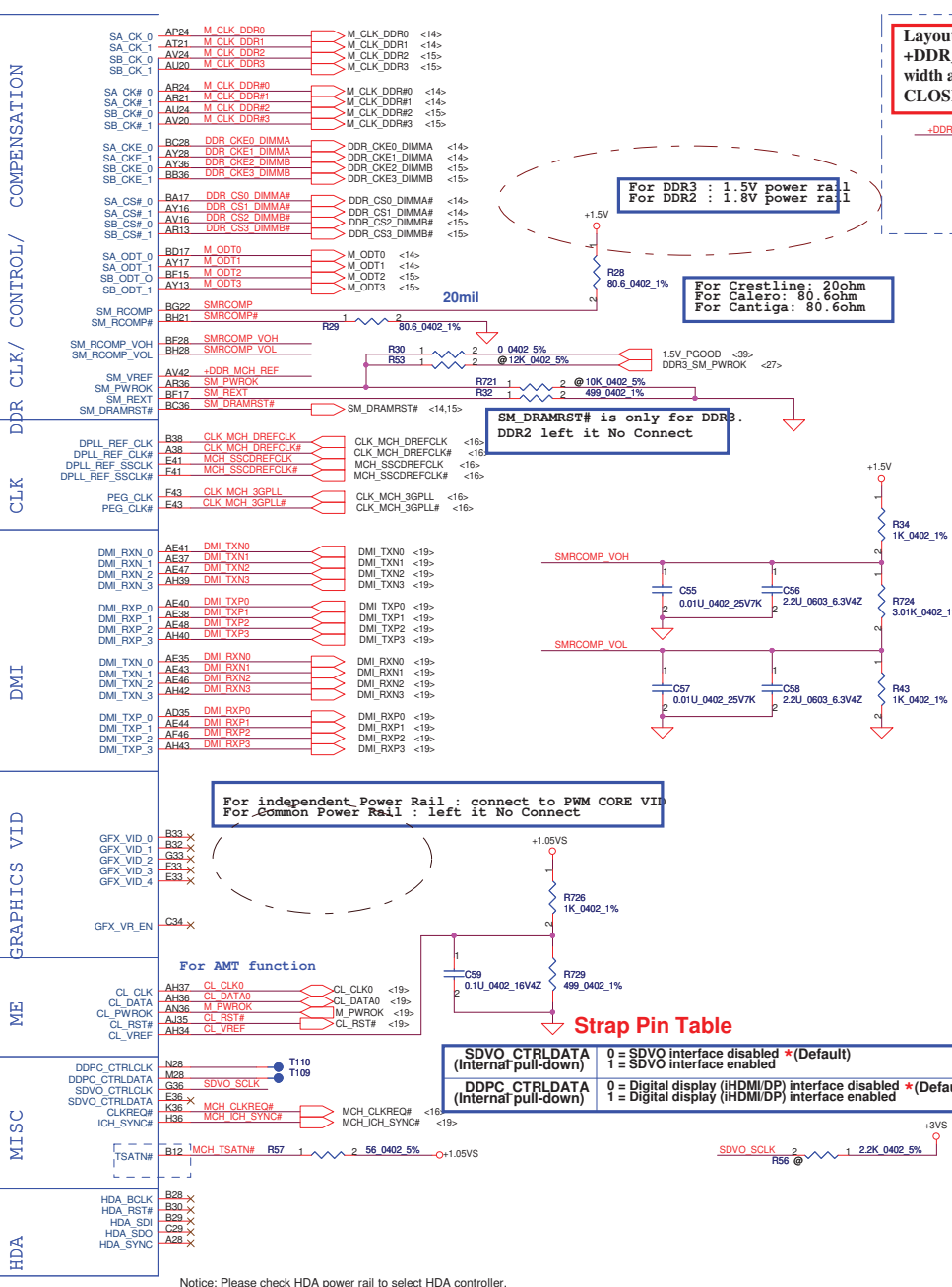
CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5 Internal pull-up	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6 Internal pull-up	0 = ITPM Host Interface is enabled can support disble by SW. 1 = ITPM Host Interface is Disabled * (Default)
CFG7 Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality * (Default)
CFG9 Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10 Internal pull-up	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12] Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation * (Default)
CFG16 Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19 Internal pull-down	0 = Normal Operation 1 = DMI Lane Reversal Enable * (Default)
CFG20 Internal pull-down (PCIe/SDVO select)	0 = Only PCIe or [SDVO/DP/HDMI] is operational. * (Default) 1 = PCIe/[SDVO/DP/HDMI] are operating simu.



09/16 Add C838 For noise



U3B	RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD10 RSVD11 RSVD12 RSVD13 RSVD14	M36 N36 R33 T33 AH9 AH10 AH12 AH13 K32 AL34 AN35 AM35 T24
B31 B2 M1	RSVD15 RSVD16 RSVD17	
AY21	RSVD20	
BG22 BF22 H118 BF18	RSVD22 RSVD23 RSVD24 RSVD25	



SM_DRAMRST# is only for DDR3. DDR2 left it No Connect

For independent Power Rail : connect to PWM CORE VDD For Common Power Rail : left it No Connect

Strap Pin Table

SDVO_CTRLDATA (Internal pull-down)	0 = SDVO interface disabled * (Default) 1 = SDVO interface enabled
DDPC_CTRLDATA (Internal pull-down)	0 = Digital display (iHDMI/DP) interface disabled * (Default) 1 = Digital display (iHDMI/DP) interface enabled

Notice: Please check HDA power rail to select HDA controller.

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<14> DDR_A_D[0..63]

U80
DDR A D0 AJ38 SA_DQ_0
DDR A D1 AJ41 SA_DQ_1
DDR A D2 AN38 SA_DQ_2
DDR A D3 AM38 SA_DQ_3
DDR A D4 AJ36 SA_DQ_4
DDR A D5 AJ40 SA_DQ_5
DDR A D6 AM44 SA_DQ_6
DDR A D7 AM42 SA_DQ_7
DDR A D8 AN43 SA_DQ_8
DDR A D9 AN44 SA_DQ_9
DDR A D10 AU40 SA_DQ_10
DDR A D11 AT38 SA_DQ_11
DDR A D12 AN41 SA_DQ_12
DDR A D13 AN39 SA_DQ_13
DDR A D14 AU44 SA_DQ_14
DDR A D15 AU42 SA_DQ_15
DDR A D16 AV39 SA_DQ_16
DDR A D17 AY44 SA_DQ_17
DDR A D18 BA40 SA_DQ_18
DDR A D19 BD43 SA_DQ_19
DDR A D20 AV41 SA_DQ_20
DDR A D21 AY43 SA_DQ_21
DDR A D22 BA41 SA_DQ_22
DDR A D23 BC40 SA_DQ_23
DDR A D24 AY37 SA_DQ_24
DDR A D25 BD38 SA_DQ_25
DDR A D26 AV37 SA_DQ_26
DDR A D27 AT36 SA_DQ_27
DDR A D28 AY38 SA_DQ_28
DDR A D29 BB38 SA_DQ_29
DDR A D30 AV36 SA_DQ_30
DDR A D31 AW36 SA_DQ_31
DDR A D32 BD13 SA_DQ_32
DDR A D33 AU11 SA_DQ_33
DDR A D34 BC11 SA_DQ_34
DDR A D35 BA12 SA_DQ_35
DDR A D36 AU13 SA_DQ_36
DDR A D37 AV13 SA_DQ_37
DDR A D38 BD12 SA_DQ_38
DDR A D39 BC12 SA_DQ_39
DDR A D40 BB9 SA_DQ_40
DDR A D41 BA9 SA_DQ_41
DDR A D42 AU10 SA_DQ_42
DDR A D43 AV9 SA_DQ_43
DDR A D44 BA11 SA_DQ_44
DDR A D45 BD9 SA_DQ_45
DDR A D46 AY8 SA_DQ_46
DDR A D47 BA6 SA_DQ_47
DDR A D48 AV9 SA_DQ_48
DDR A D49 AV7 SA_DQ_49
DDR A D50 AT9 SA_DQ_50
DDR A D51 AN8 SA_DQ_51
DDR A D52 AU5 SA_DQ_52
DDR A D53 AU6 SA_DQ_53
DDR A D54 AT5 SA_DQ_54
DDR A D55 AN10 SA_DQ_55
DDR A D56 AM11 SA_DQ_56
DDR A D57 AM6 SA_DQ_57
DDR A D58 AJ9 SA_DQ_58
DDR A D59 AJ8 SA_DQ_59
DDR A D60 AN12 SA_DQ_60
DDR A D61 AM13 SA_DQ_61
DDR A D62 AJ11 SA_DQ_62
DDR A D63 AJ12 SA_DQ_63

DDR SYSTEM MEMORY A

SA_BS_0
SA_BS_1
SA_BS_2
SA_RAS#
SA_CAS#
SA_WE#

BD21 DDR A BS0
BG18 DDR A BS1
AT25 DDR A BS2
BB20 DDR A RAS#
BD20 DDR A CAS#
AY20 DDR A WE#

DDR_A_RAS# <14>
DDR_A_CAS# <14>
DDR_A_WE# <14>

SA_DM_0
SA_DM_1
SA_DM_2
SA_DM_3
SA_DM_4
SA_DM_5
SA_DM_6
SA_DM_7

AM37 DDR A DM0
AT41 DDR A DM1
AY41 DDR A DM2
AU39 DDR A DM3
BB12 DDR A DM4
AY5 DDR A DM5
AT7 DDR A DM6
AJ5 DDR A DM7

DDR_A_DM[0..7] <14>

SA_DQS_0
SA_DQS_1
SA_DQS_2
SA_DQS_3
SA_DQS_4
SA_DQS_5
SA_DQS_6
SA_DQS_7

AJ44 DDR A DQS0
AT44 DDR A DQS1
BA43 DDR A DQS2
BC37 DDR A DQS3
AW12 DDR A DQS4
BC8 DDR A DQS5
AJ8 DDR A DQS6
AM7 DDR A DQS7

DDR_A_DQS[0..7] <14>

SA_DQS#_0
SA_DQS#_1
SA_DQS#_2
SA_DQS#_3
SA_DQS#_4
SA_DQS#_5
SA_DQS#_6
SA_DQS#_7

AJ43 DDR A DQS#0
AT43 DDR A DQS#1
BA44 DDR A DQS#2
BD37 DDR A DQS#3
AY12 DDR A DQS#4
BD8 DDR A DQS#5
AJ9 DDR A DQS#6
AM8 DDR A DQS#7

DDR_A_MA[0..14] <14>

SA_MA_0
SA_MA_1
SA_MA_2
SA_MA_3
SA_MA_4
SA_MA_5
SA_MA_6
SA_MA_7
SA_MA_8
SA_MA_9
SA_MA_10
SA_MA_11
SA_MA_12
SA_MA_13
SA_MA_14

BA21 DDR A MA0
BC24 DDR A MA1
BA24 DDR A MA2
BH24 DDR A MA3
BC35 DDR A MA4
BA24 DDR A MA5
BD24 DDR A MA6
BC27 DDR A MA7
BF25 DDR A MA8
AW24 DDR A MA9
BC21 DDR A MA10
BH26 DDR A MA12
BH17 DDR A MA13
AY25 DDR A MA14

CANTIGA_ES_FCBGA1329
GM45@

USE
DDR B D0 AK47 SB_DQ_0
DDR B D1 AH46 SB_DQ_1
DDR B D2 AP47 SB_DQ_2
DDR B D3 AP46 SB_DQ_3
DDR B D4 AJ46 SB_DQ_4
DDR B D5 AJ48 SB_DQ_5
DDR B D6 AM48 SB_DQ_6
DDR B D7 AP48 SB_DQ_7
DDR B D8 AJ47 SB_DQ_8
DDR B D9 AU46 SB_DQ_9
DDR B D10 AY48 SB_DQ_10
DDR B D11 BA48 SB_DQ_11
DDR B D12 AT47 SB_DQ_12
DDR B D13 BA47 SB_DQ_13
DDR B D14 BA47 SB_DQ_14
DDR B D15 BC47 SB_DQ_15
DDR B D16 BC46 SB_DQ_16
DDR B D17 BC44 SB_DQ_17
DDR B D18 BC43 SB_DQ_18
DDR B D19 BF43 SB_DQ_19
DDR B D20 BE45 SB_DQ_20
DDR B D21 BD41 SB_DQ_21
DDR B D22 BF40 SB_DQ_22
DDR B D23 BF41 SB_DQ_23
DDR B D24 BG38 SB_DQ_24
DDR B D25 BF38 SB_DQ_25
DDR B D26 BH35 SB_DQ_26
DDR B D27 BC35 SB_DQ_27
DDR B D28 BH40 SB_DQ_28
DDR B D29 BG39 SB_DQ_29
DDR B D30 BG34 SB_DQ_30
DDR B D31 BH34 SB_DQ_31
DDR B D32 BG12 SB_DQ_32
DDR B D33 BG12 SB_DQ_33
DDR B D34 BH11 SB_DQ_34
DDR B D35 BG8 SB_DQ_35
DDR B D36 BH12 SB_DQ_36
DDR B D37 BE11 SB_DQ_37
DDR B D38 BF8 SB_DQ_38
DDR B D39 BG7 SB_DQ_39
DDR B D40 BC5 SB_DQ_40
DDR B D41 BC6 SB_DQ_41
DDR B D42 AY3 SB_DQ_42
DDR B D43 AY1 SB_DQ_43
DDR B D44 BF6 SB_DQ_44
DDR B D45 BF5 SB_DQ_45
DDR B D46 BA1 SB_DQ_46
DDR B D47 BC3 SB_DQ_47
DDR B D48 AV2 SB_DQ_48
DDR B D49 AU3 SB_DQ_49
DDR B D50 AR3 SB_DQ_50
DDR B D51 AN2 SB_DQ_51
DDR B D52 AY2 SB_DQ_52
DDR B D53 AV1 SB_DQ_53
DDR B D54 AP3 SB_DQ_54
DDR B D55 AR1 SB_DQ_55
DDR B D56 AL1 SB_DQ_56
DDR B D57 AL2 SB_DQ_57
DDR B D58 AJ1 SB_DQ_58
DDR B D59 AH1 SB_DQ_59
DDR B D60 AM2 SB_DQ_60
DDR B D61 AM3 SB_DQ_61
DDR B D62 AH3 SB_DQ_62
DDR B D63 AJ3 SB_DQ_63

DDR_B_RAS# <15>
DDR_B_CAS# <15>
DDR_B_WE# <15>

DDR SYSTEM MEMORY B

SB_BS_0
SB_BS_1
SB_BS_2
SB_RAS#
SB_CAS#
SB_WE#

BC16 DDR B BS0
BB17 DDR B BS1
BB33 DDR B BS2
AU17 DDR B RAS#
BG16 DDR B CAS#
BF14 DDR B WE#

DDR_B_RAS# <15>
DDR_B_CAS# <15>
DDR_B_WE# <15>

SB_DM_0
SB_DM_1
SB_DM_2
SB_DM_3
SB_DM_4
SB_DM_5
SB_DM_6
SB_DM_7

AM7 DDR B DM0
AY47 DDR B DM1
BD40 DDR B DM2
BF35 DDR B DM3
BG11 DDR B DM4
BA3 DDR B DM5
AP17 DDR B DM6
AK2 DDR B DM7

DDR_B_DM[0..7] <15>

SB_DQS_0
SB_DQS_1
SB_DQS_2
SB_DQS_3
SB_DQS_4
SB_DQS_5
SB_DQS_6
SB_DQS_7

AL47 DDR B DQS0
AV48 DDR B DQS1
BG41 DDR B DQS2
BG37 DDR B DQS3
BH9 DDR B DQS4
BB2 DDR B DQS5
AU1 DDR B DQS6
AN6 DDR B DQS7

DDR_B_DQS[0..7] <15>

SB_DQS#_0
SB_DQS#_1
SB_DQS#_2
SB_DQS#_3
SB_DQS#_4
SB_DQS#_5
SB_DQS#_6
SB_DQS#_7

AL46 DDR B DQS#0
AV47 DDR B DQS#1
BH41 DDR B DQS#2
BH7 DDR B DQS#3
BG9 DDR B DQS#4
BC2 DDR B DQS#5
AT2 DDR B DQS#6
AN6 DDR B DQS#7

DDR_B_DQS#[0..7] <15>

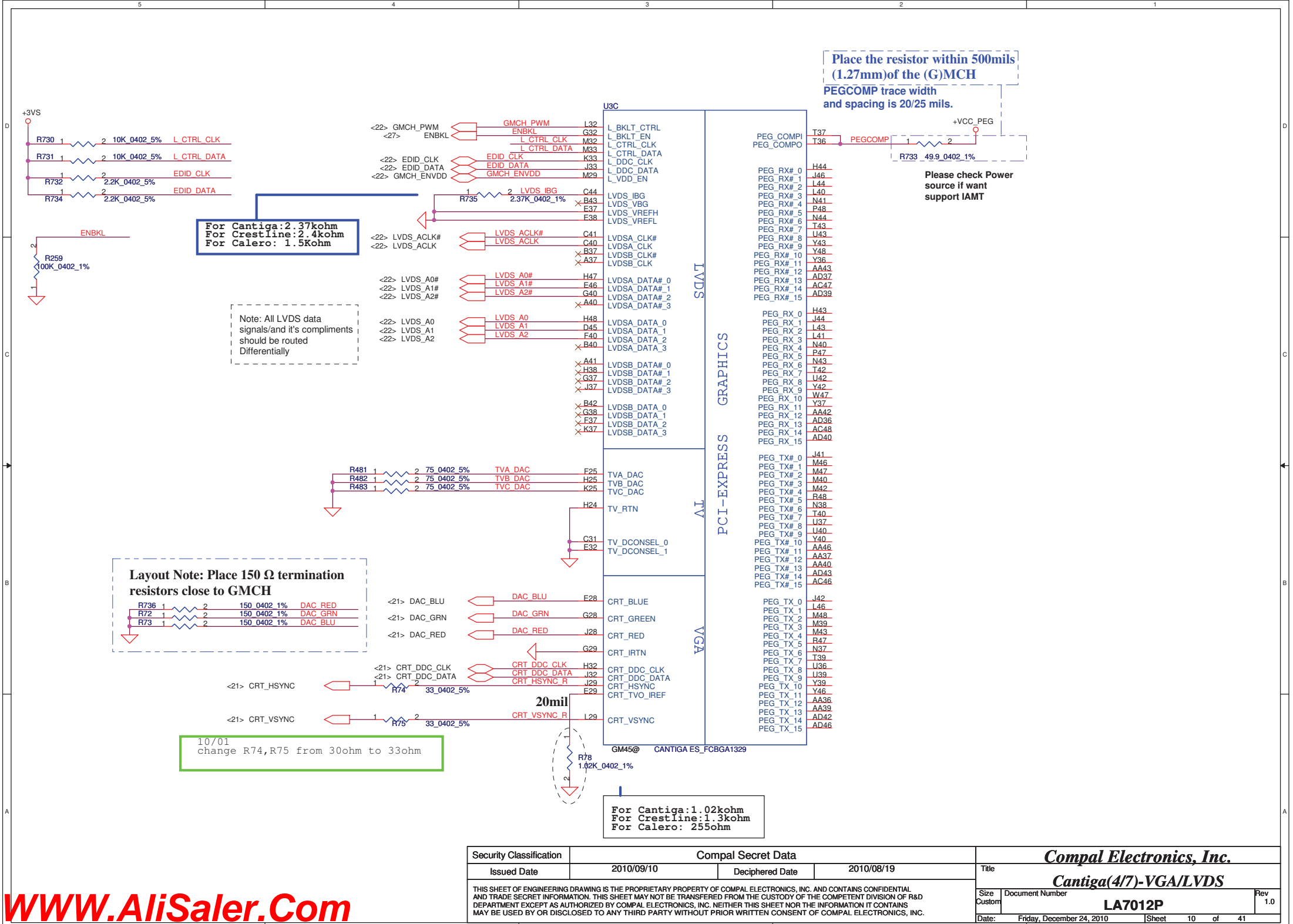
SB_MA_0
SB_MA_1
SB_MA_2
SB_MA_3
SB_MA_4
SB_MA_5
SB_MA_6
SB_MA_7
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SB_MA_9
SB_MA_10
SB_MA_11
SB_MA_12
SB_MA_13
SB_MA_14

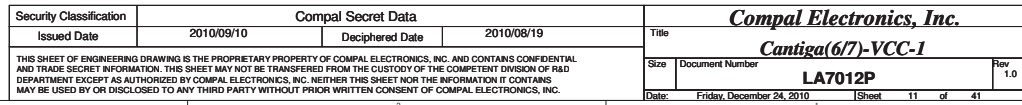
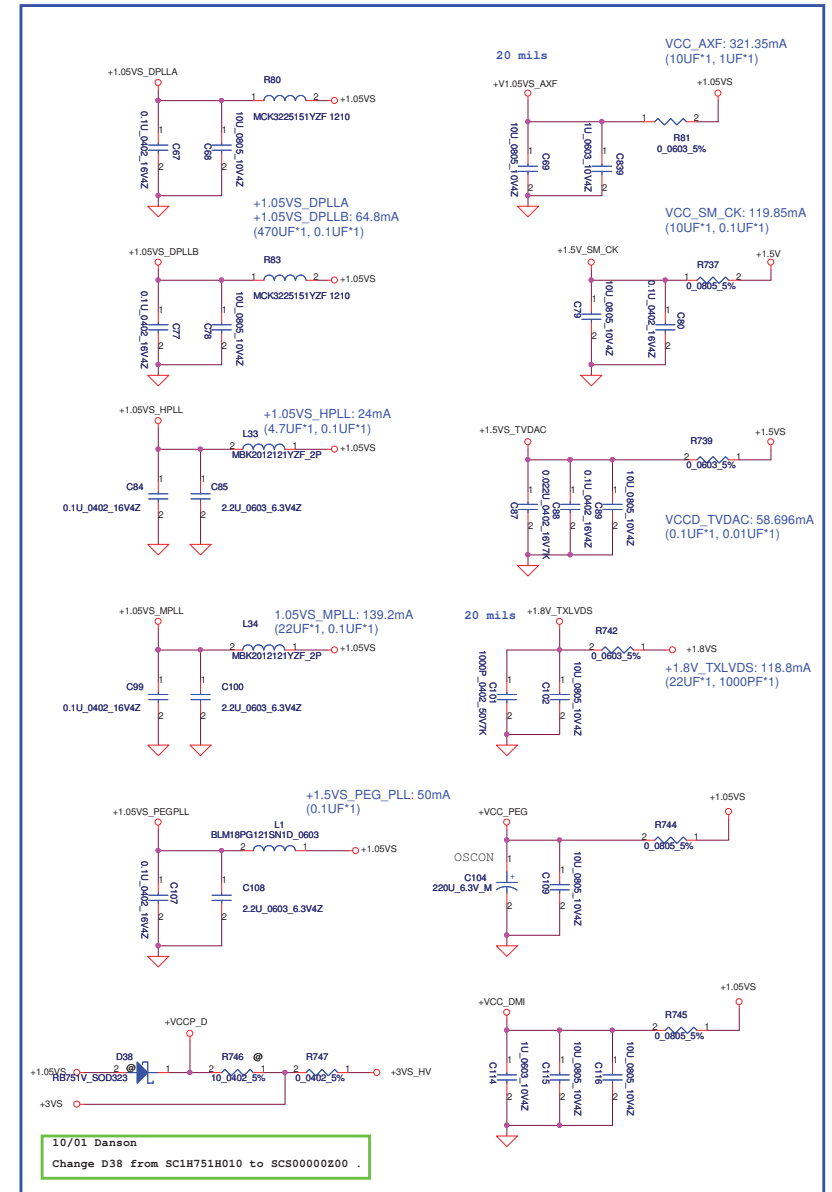
AV17 DDR B MA0
BA25 DDR B MA1
BC25 DDR B MA2
AU25 DDR B MA3
AW25 DDR B MA4
BB28 DDR B MA5
AU28 DDR B MA6
AW28 DDR B MA7
AT33 DDR B MA8
BD33 DDR B MA9
BB16 DDR B MA10
AW33 DDR B MA11
AY34 DDR B MA12
BH15 DDR B MA13
AU33 DDR B MA14

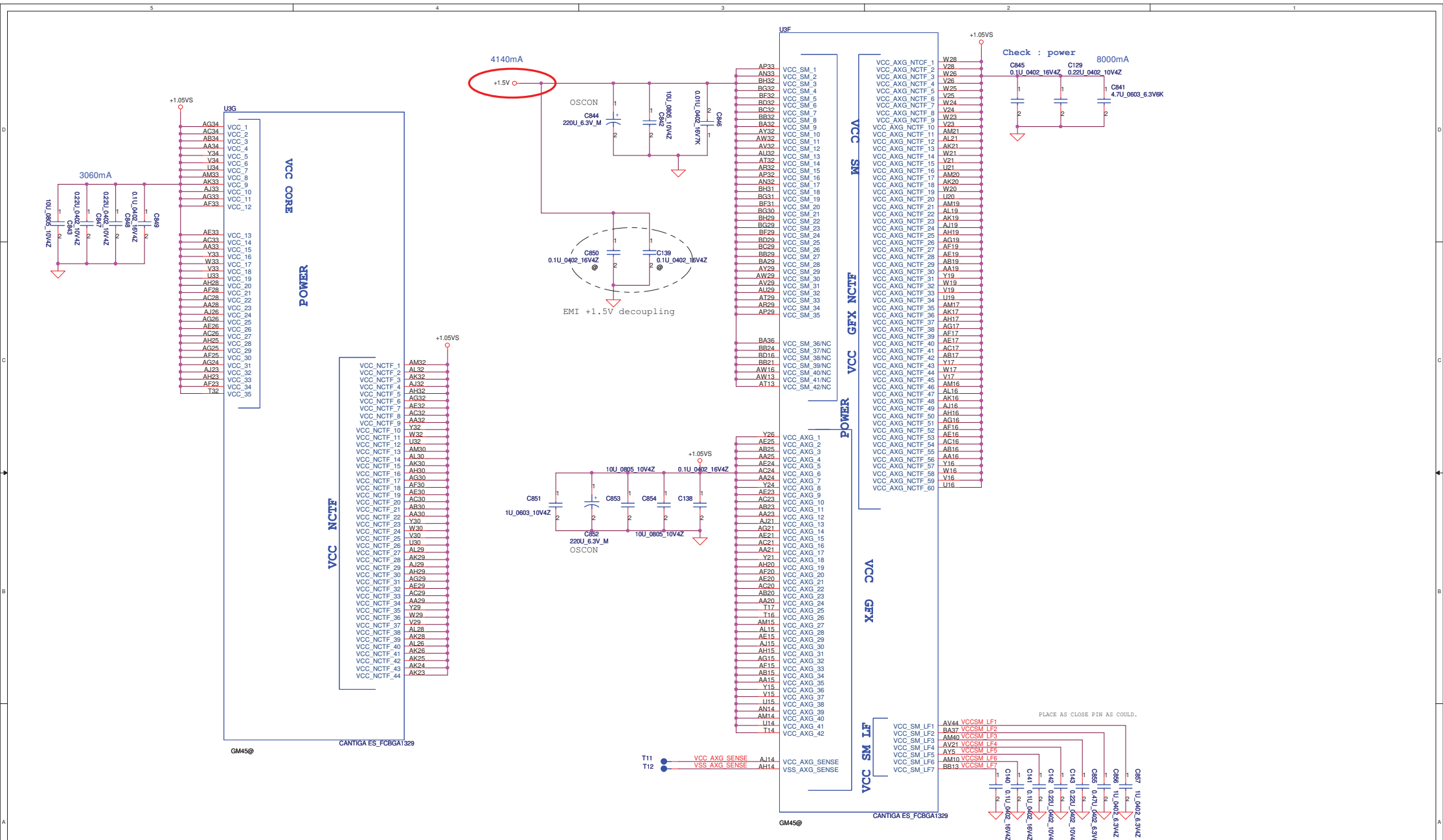
DDR_B_MA[0..14] <15>

CANTIGA_ES_FCBGA1329
GM45@

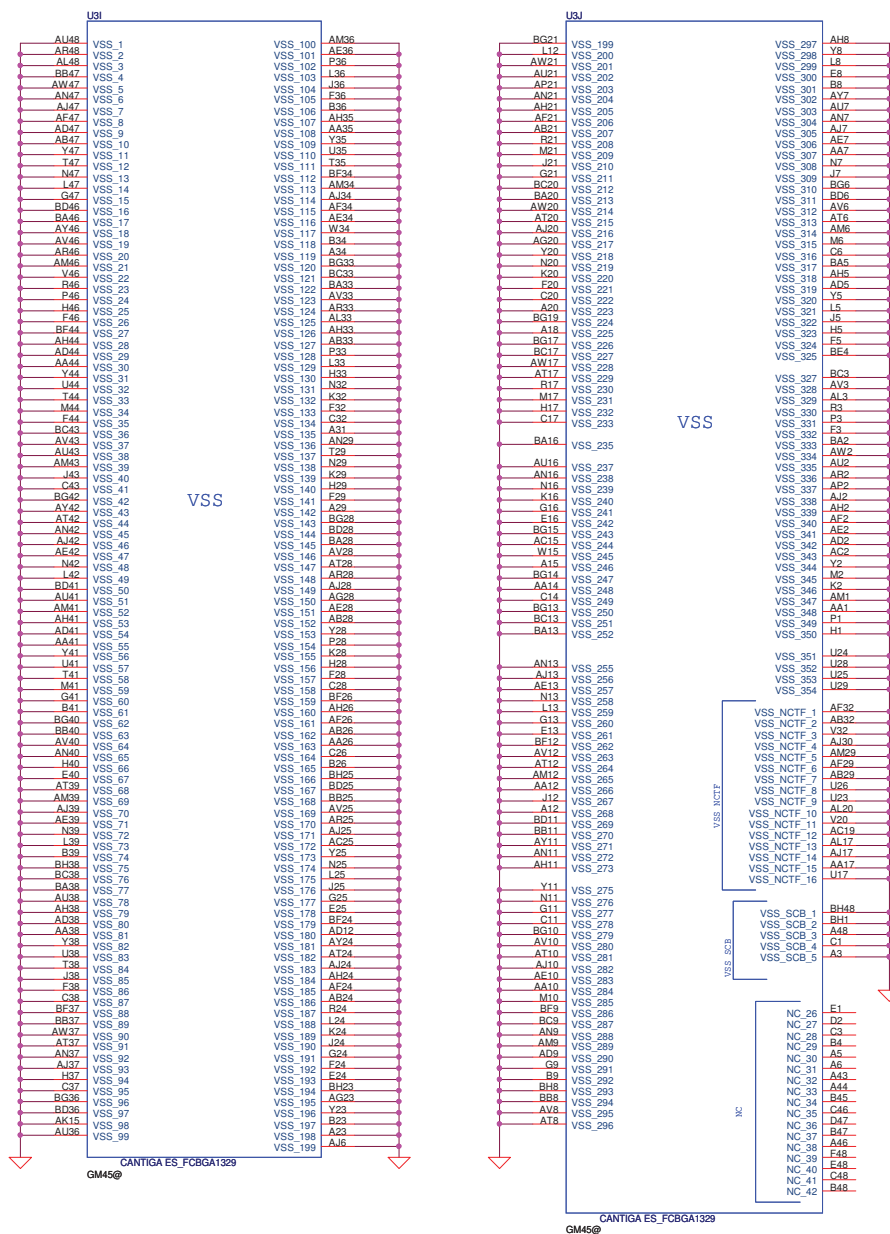
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Issued Date	2010/09/10	Deciphered Date	2010/08/19	Compal Electronics, Inc.	
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				LA7012P	1.0
				Date: Friday, December 24, 2010	Sheet 9 of 41







Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	
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Size	Document Number	LA7012P		Rev	1.0
Date:	Friday, December 24, 2010	Sheet	12	of	41



Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		2010/09/10	
2010/09/10		2010/08/19		2010/08/19	
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Sheet		13		of 41	

Compal Electronics, Inc.
Cantiga(7/7)-GND

LA7012P

Size

Custom

Date:

Friday, December 24, 2010

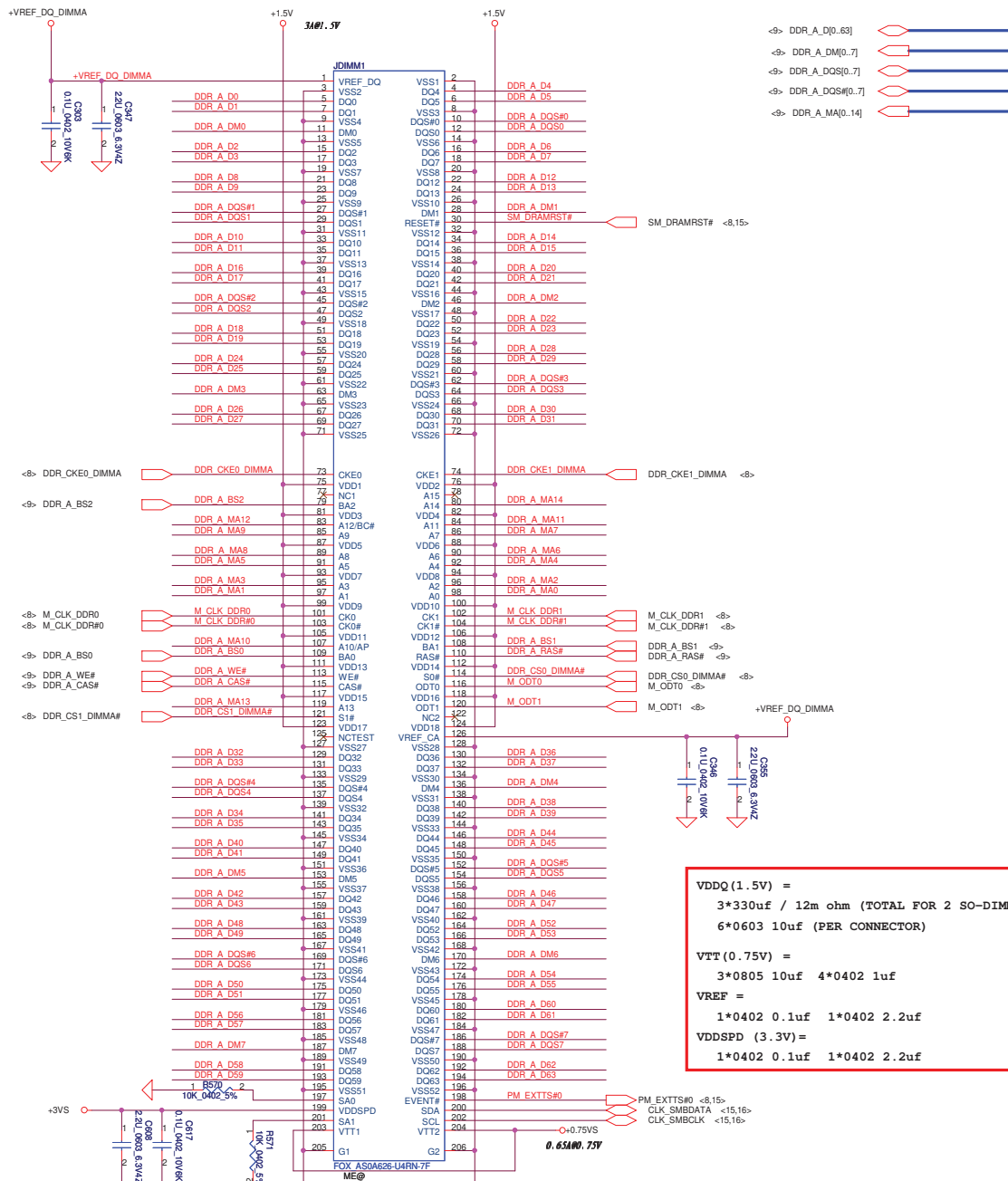
Sheet

13

of 41

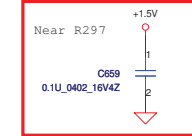
Rev

1.0



- <-> DDR_A_D[0..63]
- <-> DDR_A_DM[0..7]
- <-> DDR_A_DQS[0..7]
- <-> DDR_A_DQS# [0..7]
- <-> DDR_A_MA[0..14]

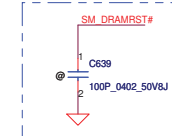
Pre MP ADD for ESD solution



For Arranale only +VREF_DQ_DIMMA supply from a external 1.5V voltage divide circuit.

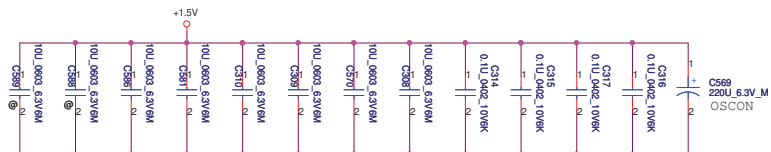
07/17/2009

Place closely pin JDIMM1.30



1224 Change C639 to @ for download image fail issue

Layout Note:
Place near DIMM

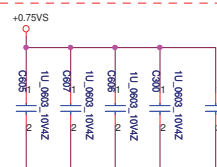


VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VREF =
1*0402 0.1uf 1*0402 2.2uf

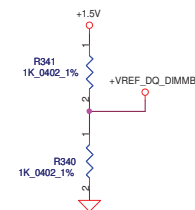
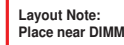
VDDSPD (3.3V) =
1*0402 0.1uf 1*0402 2.2uf



DDR3 SO-DIMM A H=4mm Reverse type

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				DDR3 SO-DIMM A	
				Size	Rev
				Customer	1.0
				LA7012P	
				Date	Friday, December 24, 2010
				Sheet	14 of 41

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07/17/2009

1224 Change C640 to @ for download image fail issue

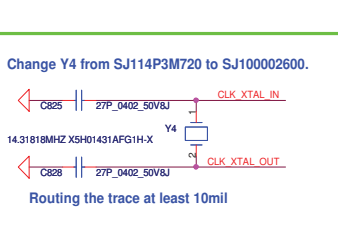
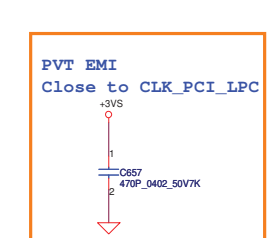
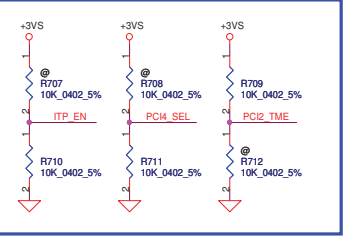
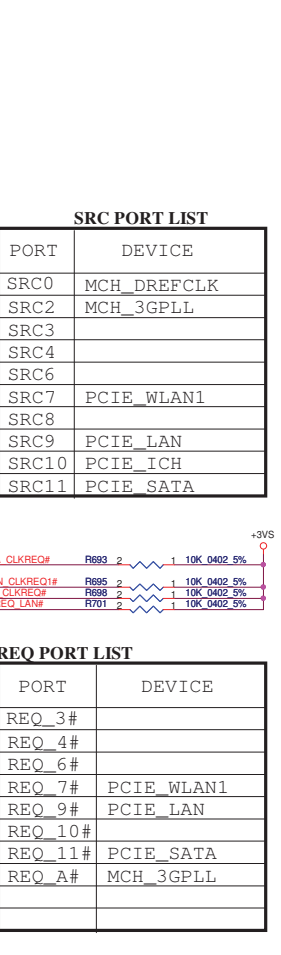
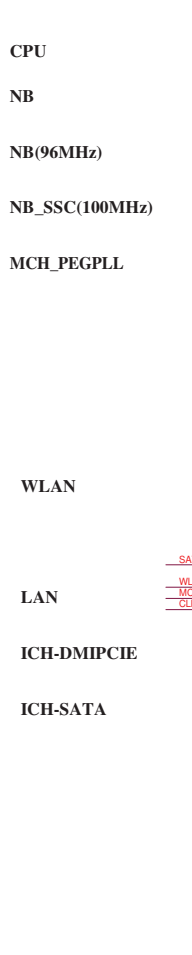
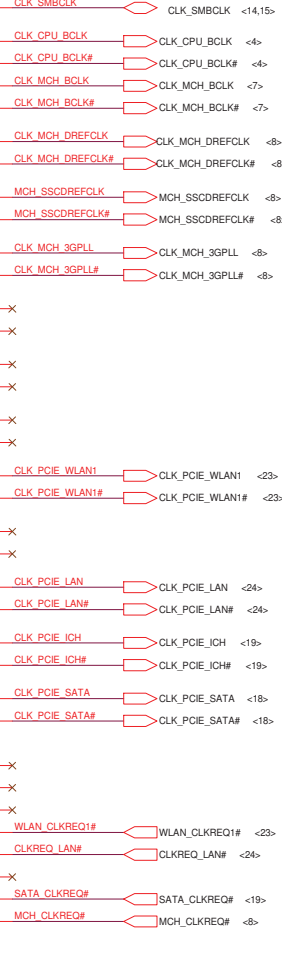
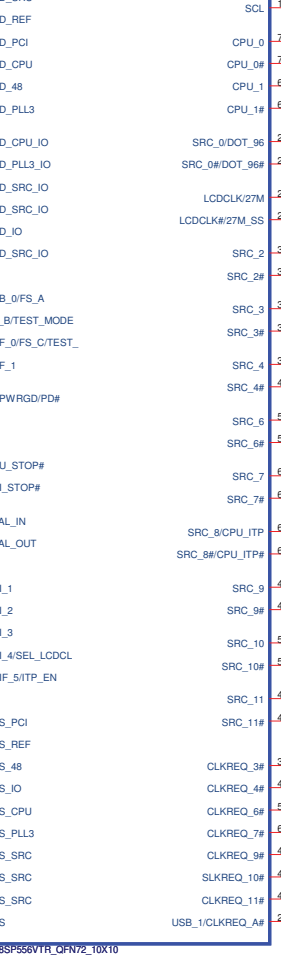
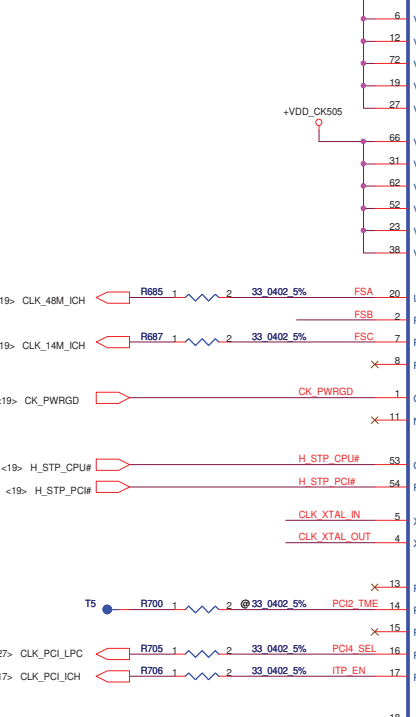
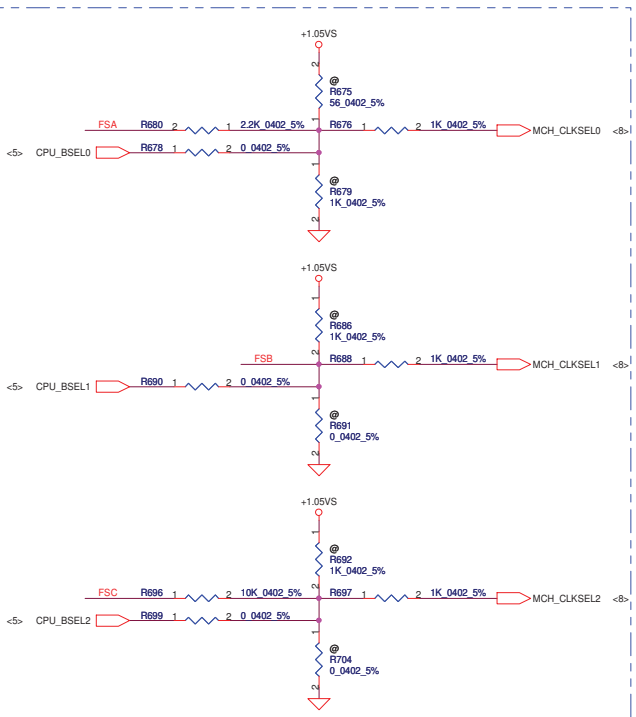
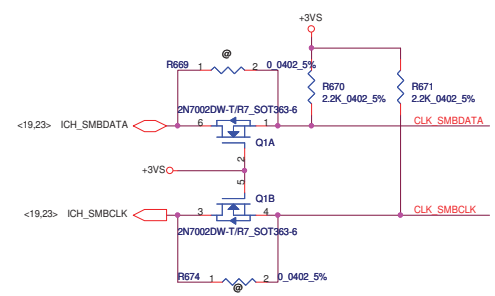
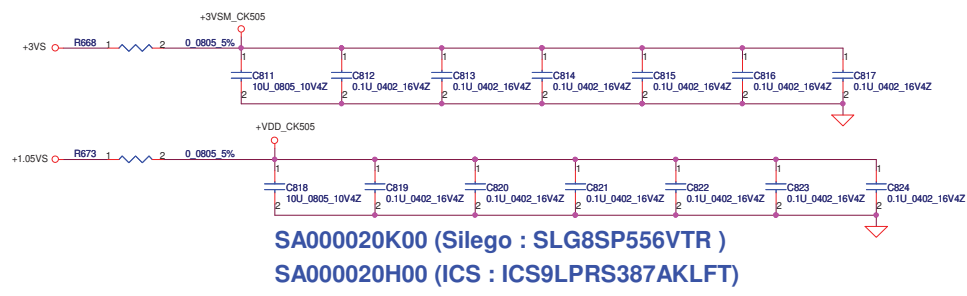
```
VTT (0.75V) =
    3*0805 10uf  4*0402 1uf

    1*0402 0.1uf  1*0402 2.2uf
VDDSPD (3.3V)=
    1*0402 0.1uf  1*0402 2.2uf
```

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Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> DDRIII SO-DIMM B	
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				Custom	1.0
				Document Number	
				LA7012P	
				Date	Friday, December 24, 2010
				Sheet	15 of 41

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



For ITP_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

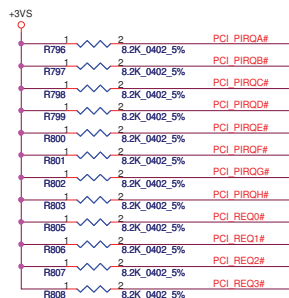
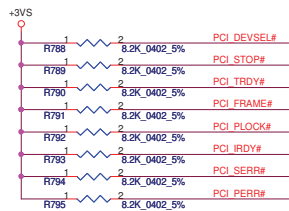
PVT EMI
Close to CLK_PCI_LPC

Change Y4 from SJ114P3M720 to SJ100002600.
14.31818MHz XSH01431AFGIH-X
Routing the trace at least 10mil

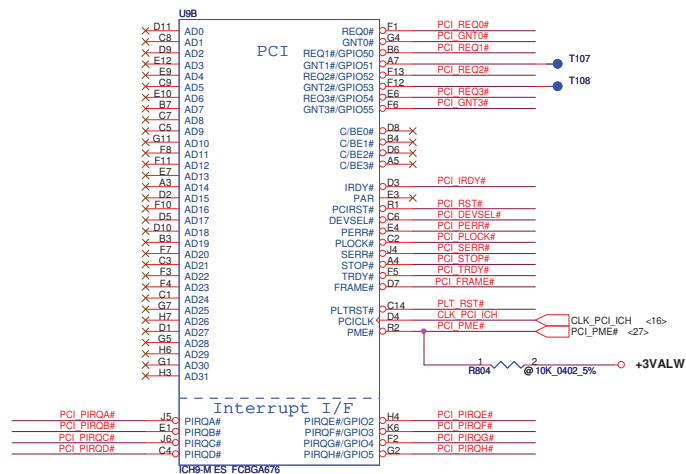
SRC PORT LIST	
PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	
SRC4	
SRC6	
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

REQ PORT LIST	
PORT	DEVICE
REQ_3#	
REQ_4#	
REQ_6#	
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

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Size Custom		Date: Friday, December 24, 2010		Rev 1.0	
		Sheet 16 of 41			



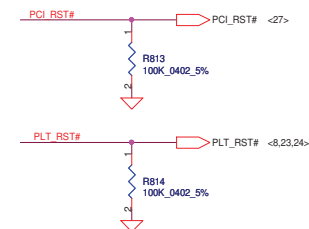
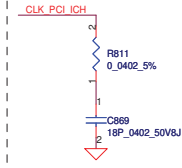
A16 Swap Override Strap	
PCI_GNT#3	Low = A16 swap override Enable High = Default*



09/16 Add C858 For ESD
Place closely pin C14

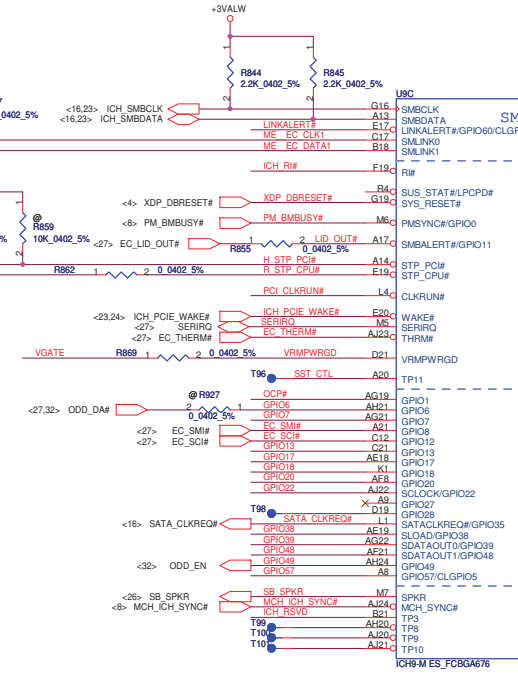
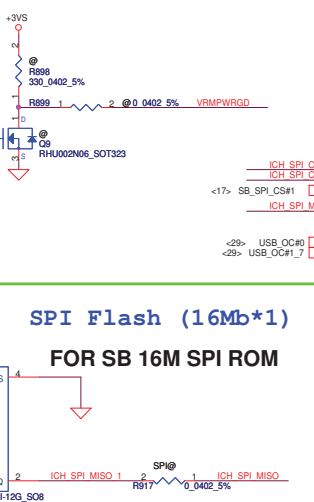
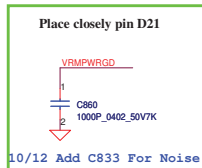
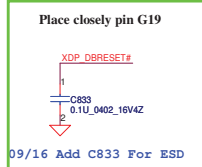
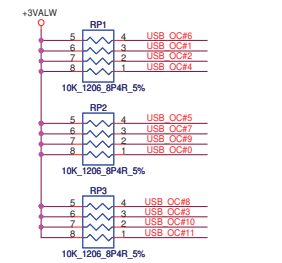
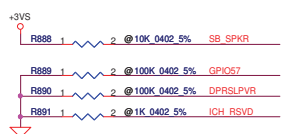
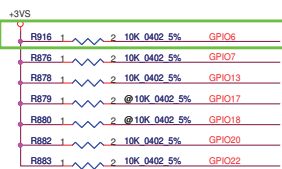
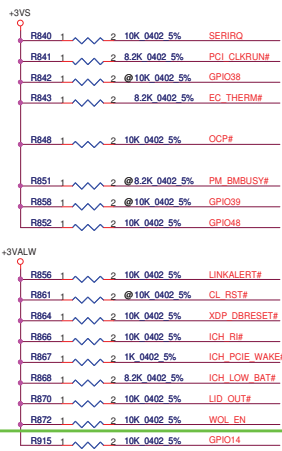


Place closely pin D4



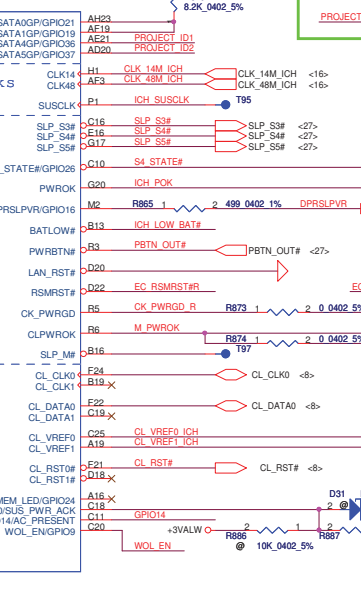
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

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				Date: Friday, December 24, 2010	Sheet 17 of 41

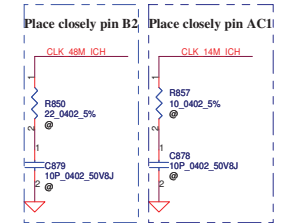
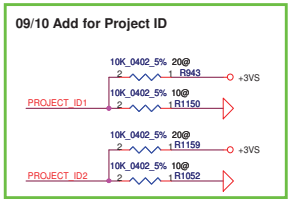


USB
SMB
clocks
S4_STATE#
DPRSLPVR
BATLOW#
PWRBTN#
RSMRST#
CK_PWRGD
SLP_M#
CL_CLK#
CL_DATA#
CL_VREF#
CL_RST#
MEM_LED#
GPIO10#
WOL_EN

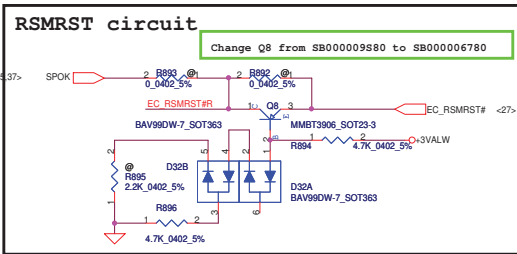
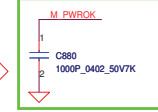
Sys / GPIO
Power Mgt
Controller Link
MISC



10/01
Change D31 from SC1H751H010 to SC5000000200



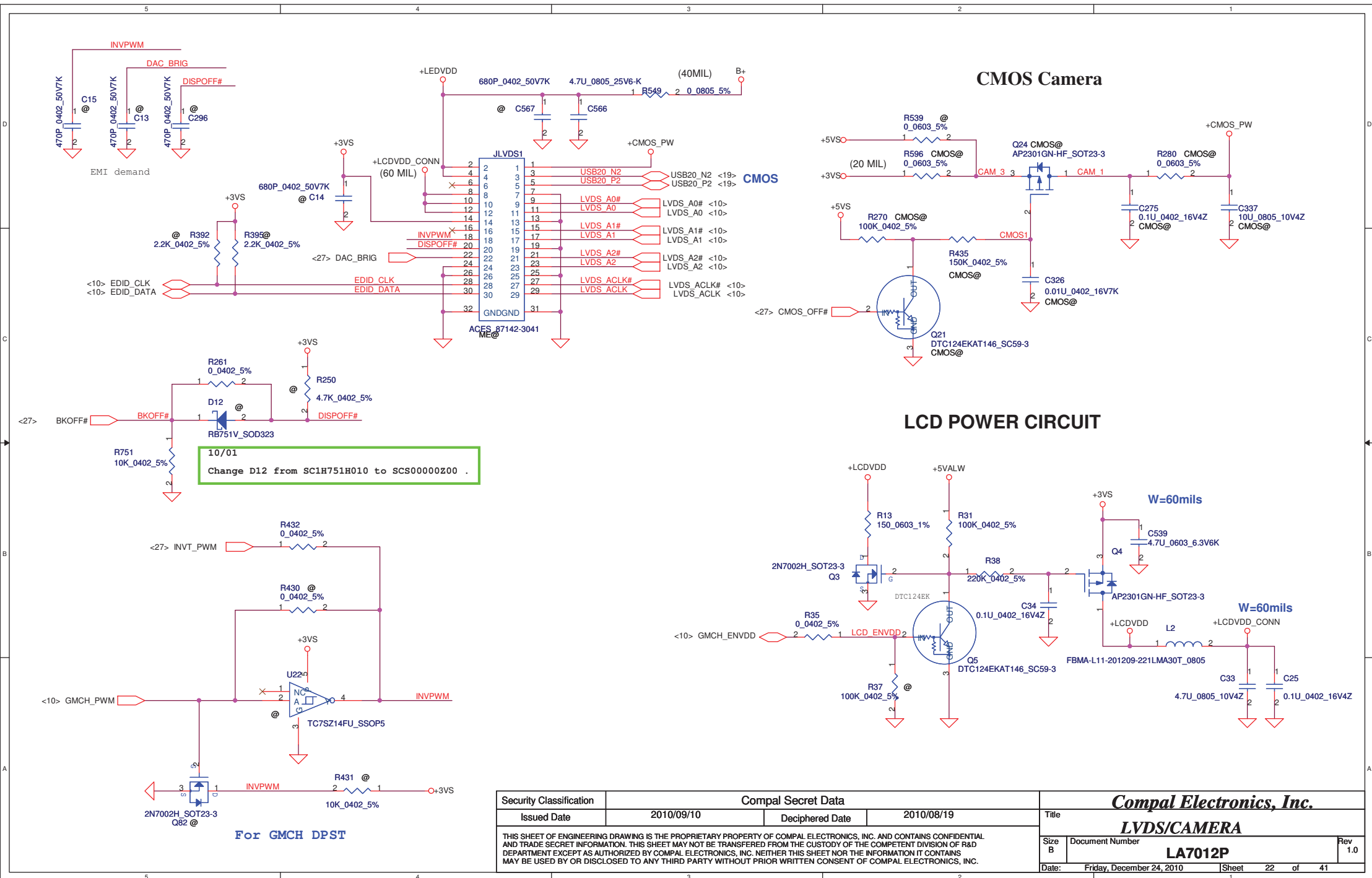
10/15 Change C880 from 100P to 1000P for noise.



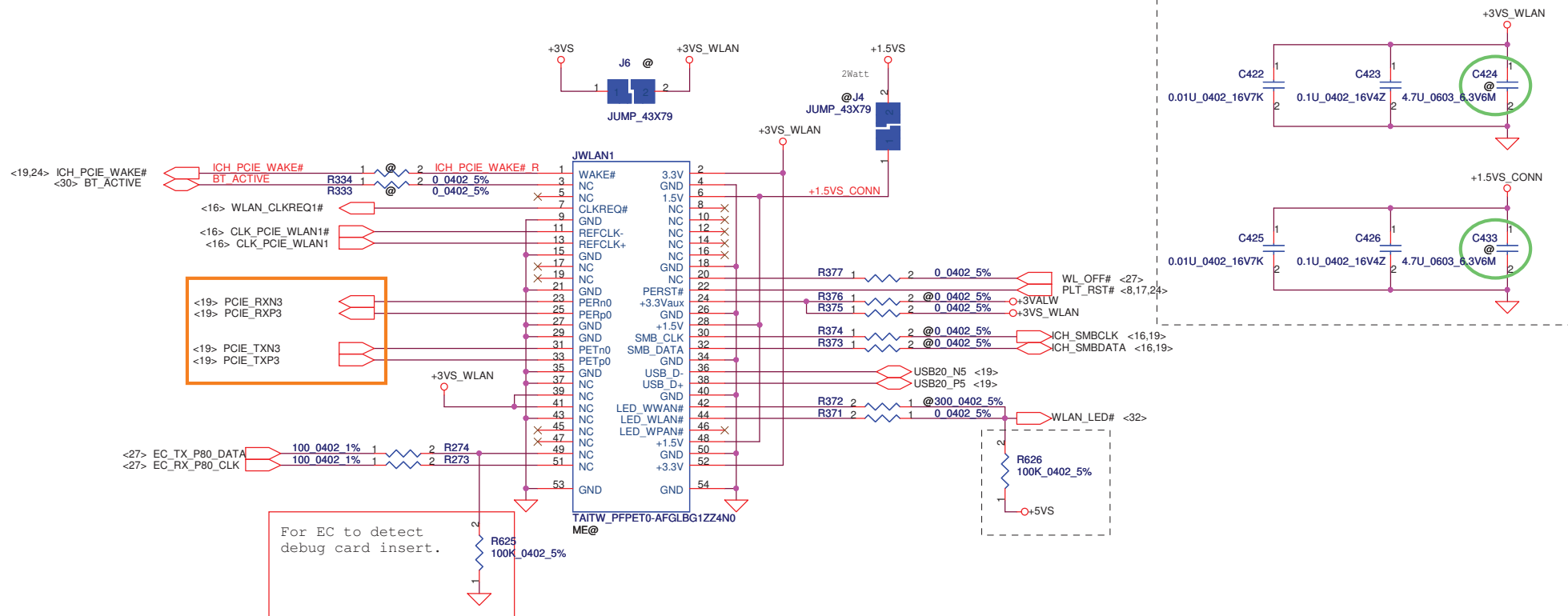
PCIE PORT LIST	
PORT	DEVICE
1	LAN
2	
3	WLAN
4	
5	
6	

USB PORT LIST	
PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	
4	CARD READER
5	WIRELESS
6	BT
7	LEFT SIDE
8	
9	
10	
11	

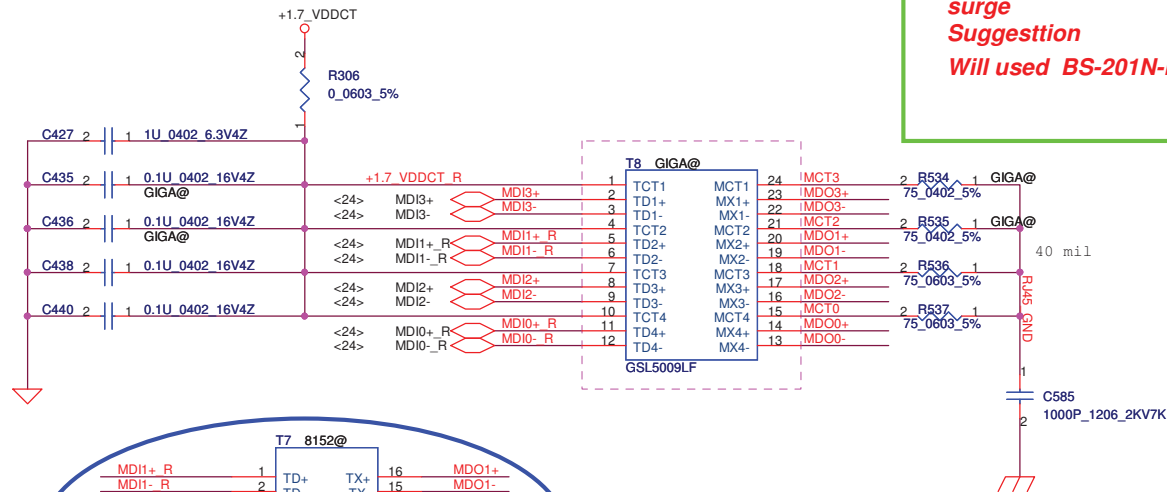




Mini-Express Card for WLAN(Half)

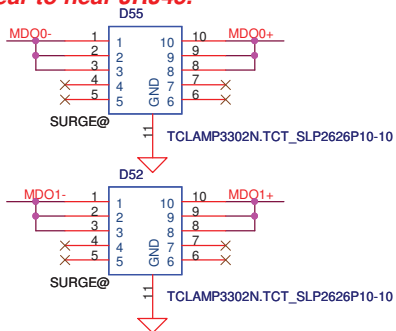


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				Size	Rev
				Document Number	1.0
				LA7012P	
				Date:	Friday, December 24, 2010
				Sheet	23 of 41

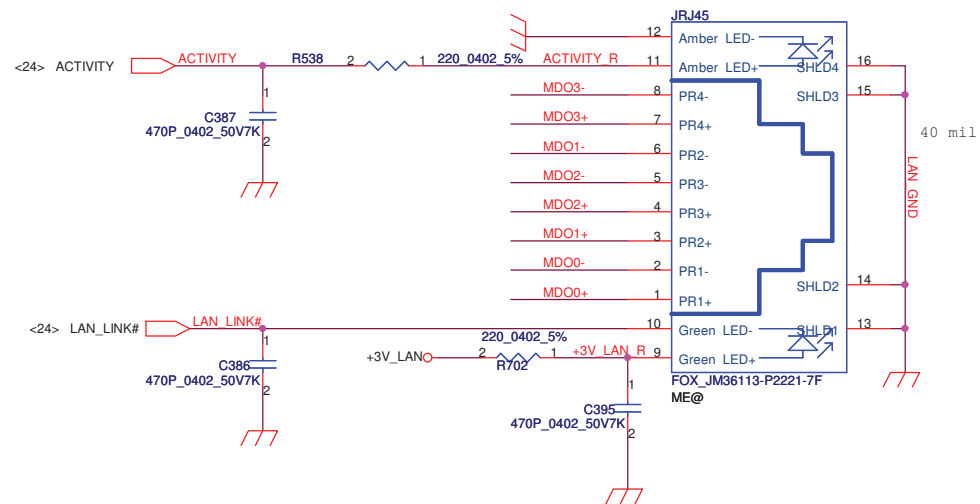
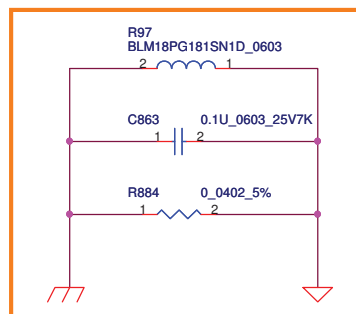


12/13 PreMP Add it for avoid to be struck by lightning

Near to near JRJ45.

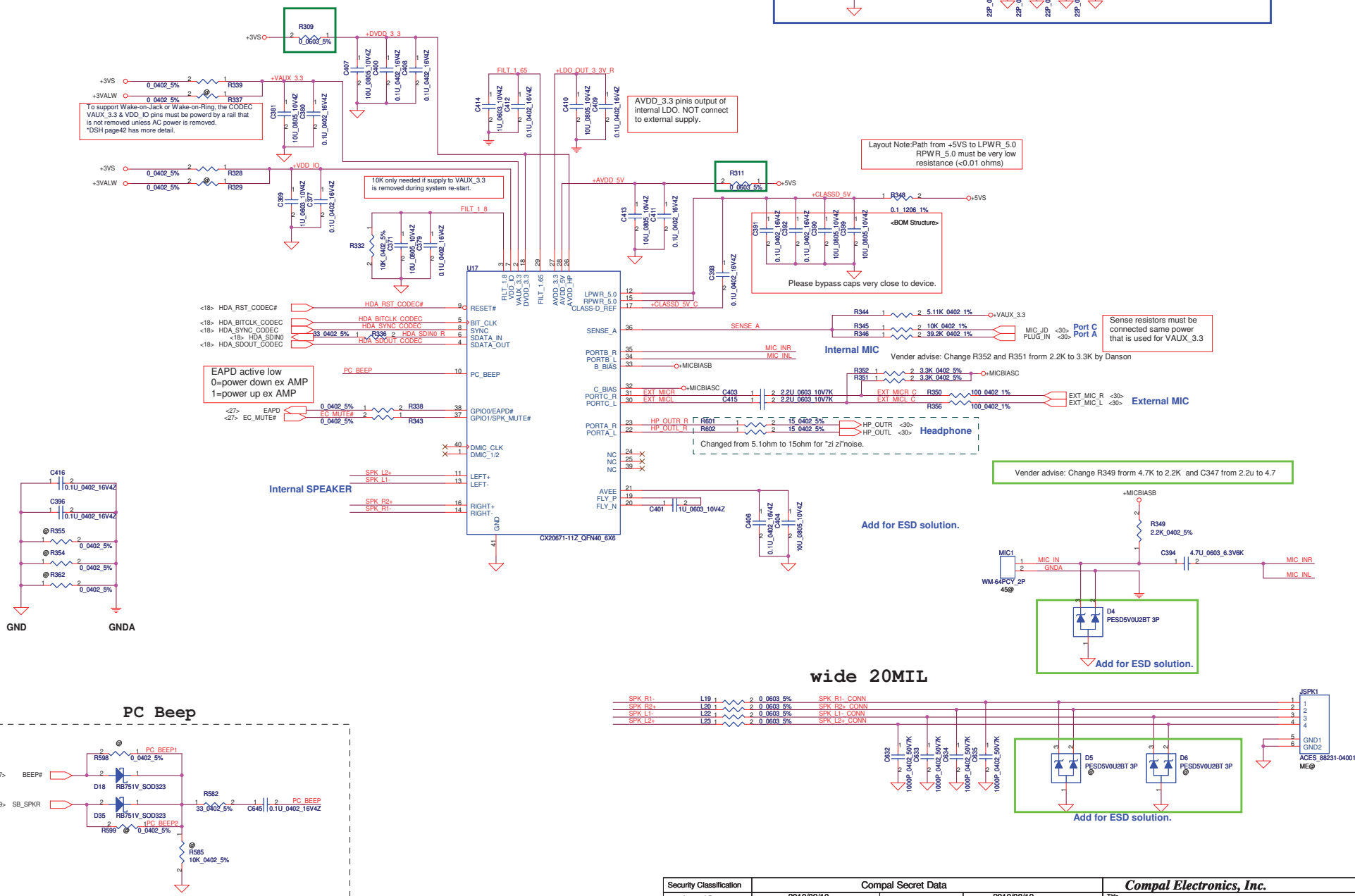
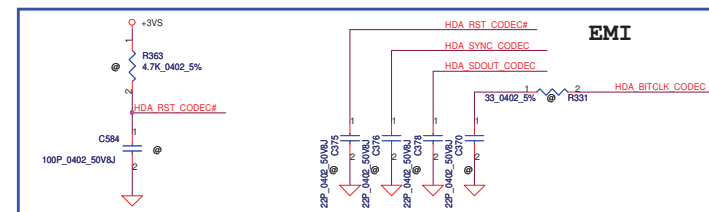


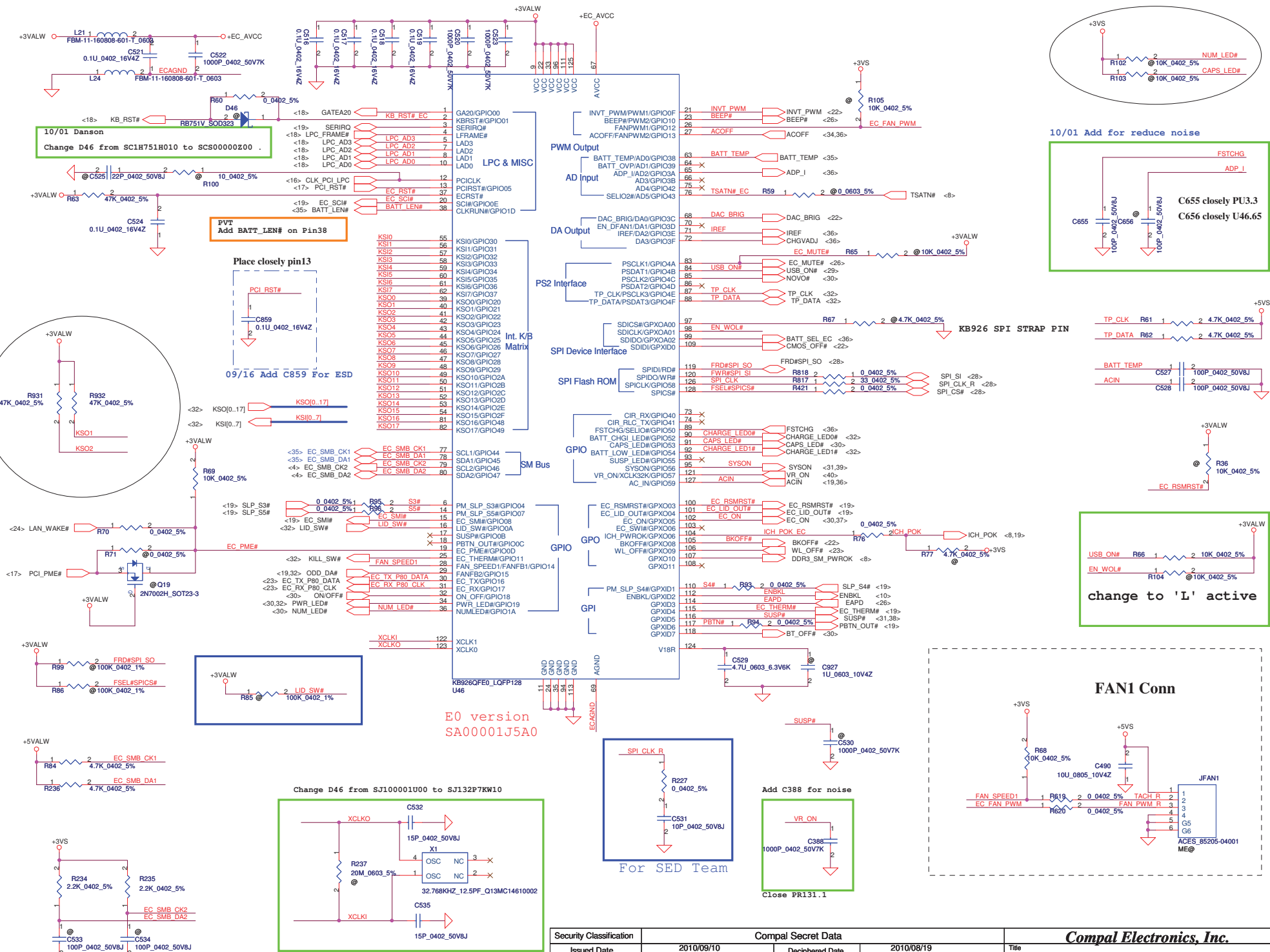
PVT Add EMI solution.



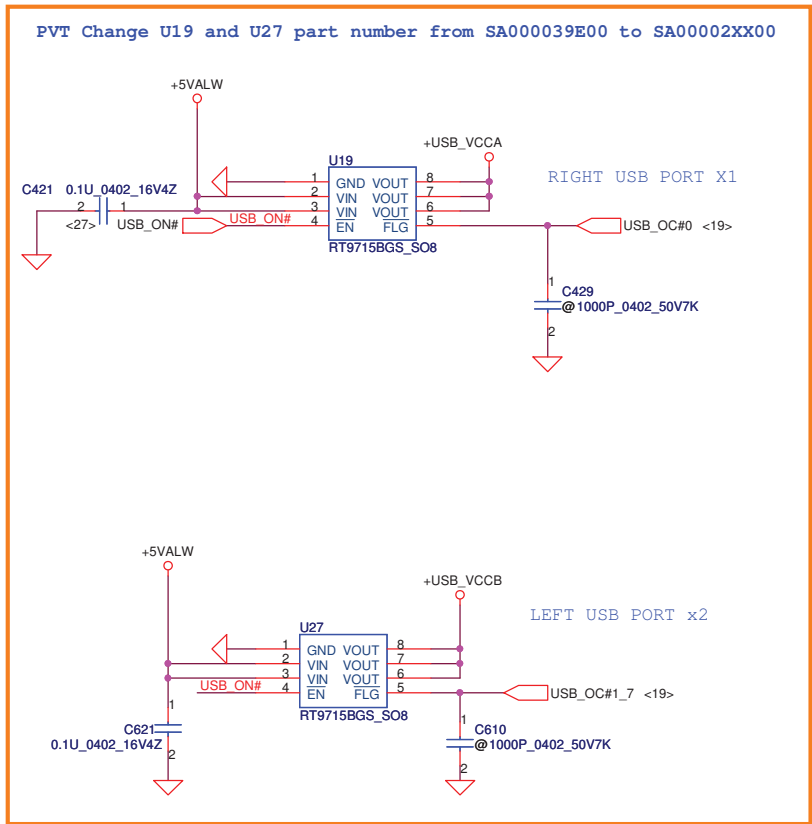
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Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	
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CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

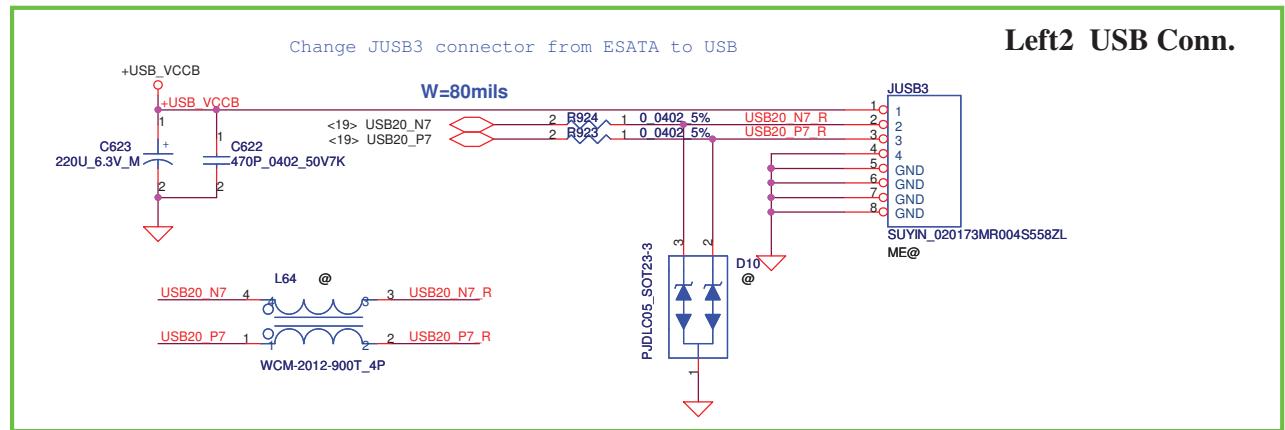
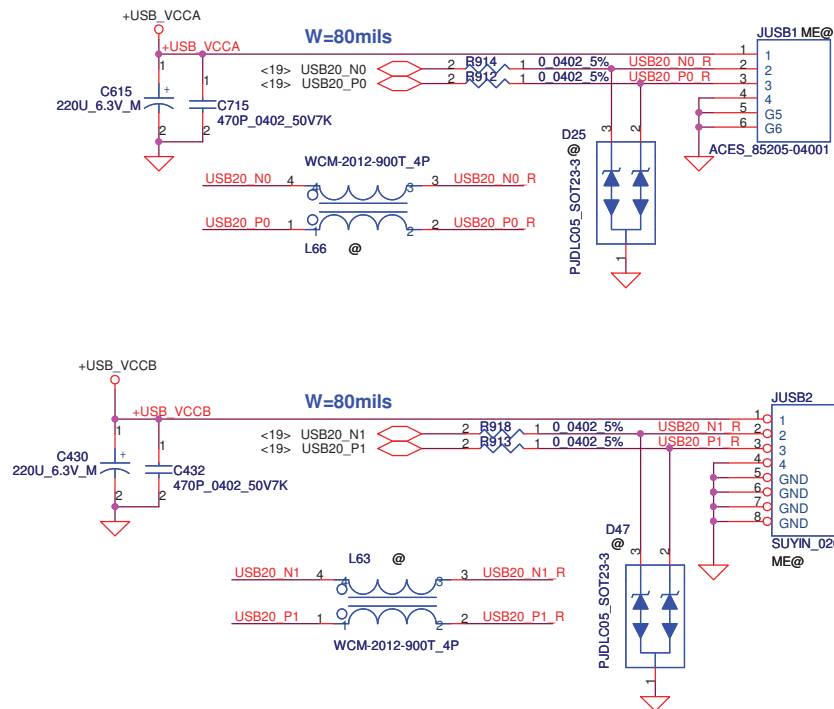
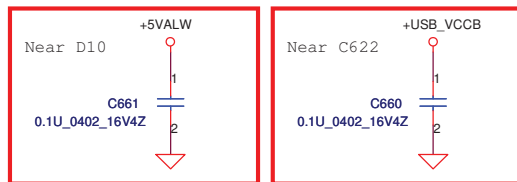




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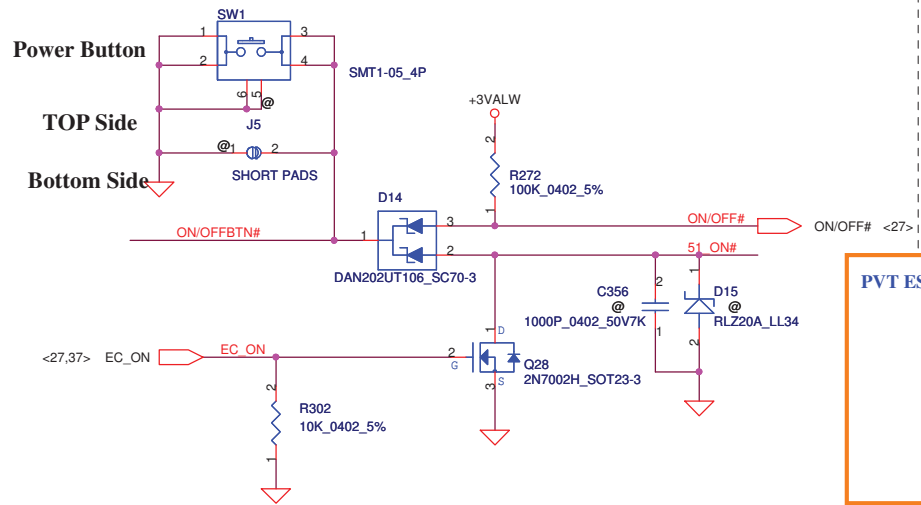


Pre MP ADD for ESD solution

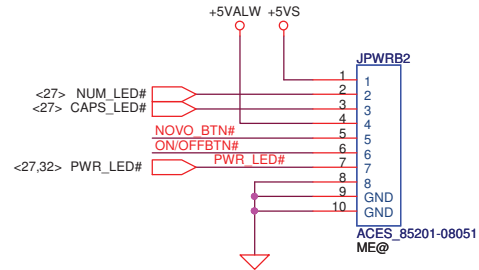


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Size	B	Document Number	LA7012P		Rev
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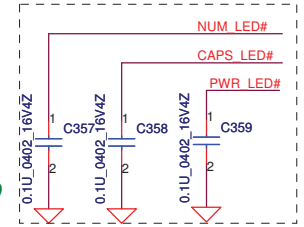
ON/OFF switch



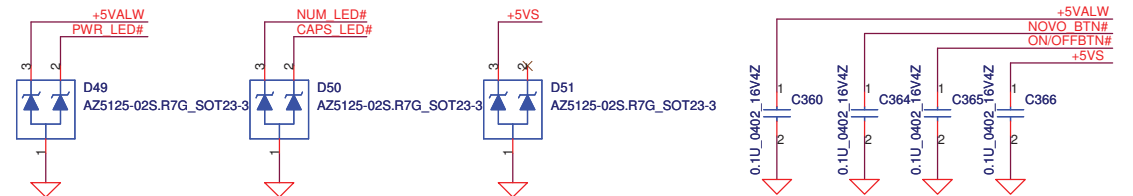
Power Bottom Board Conn. 8pin



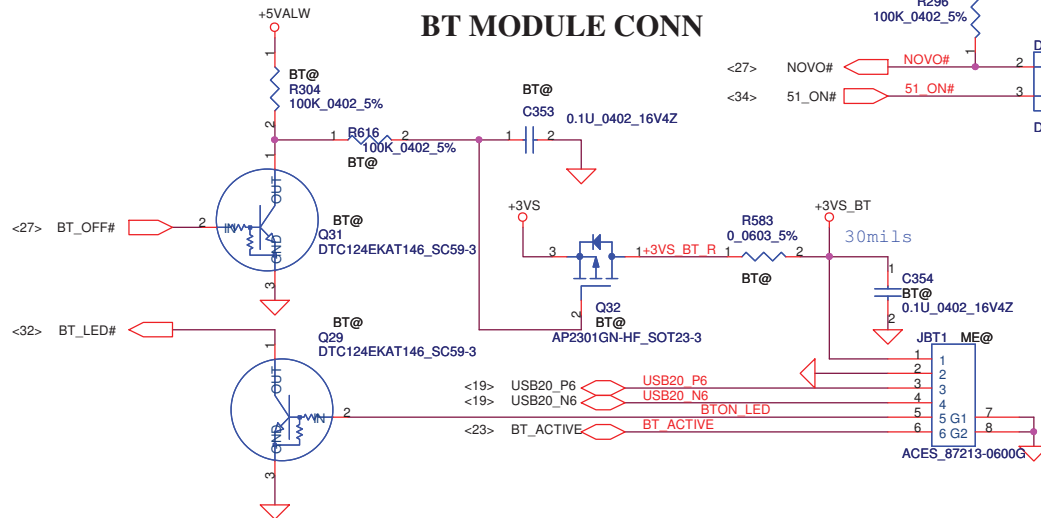
EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00



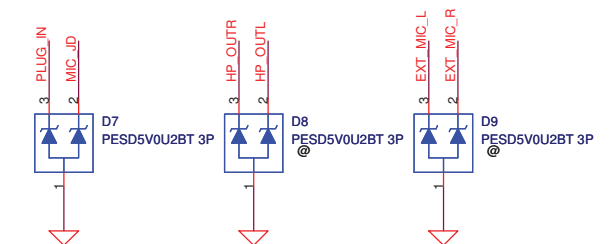
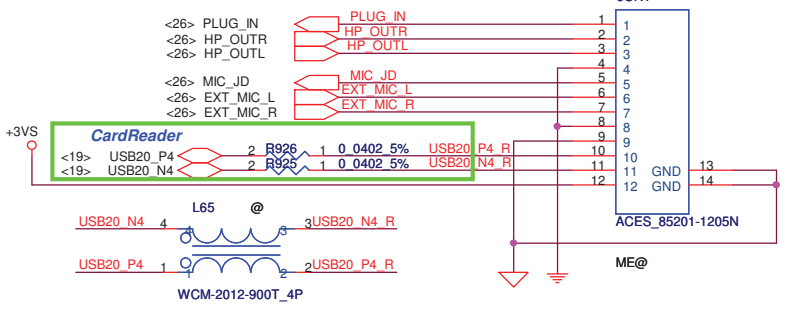
PVT ESD solution.



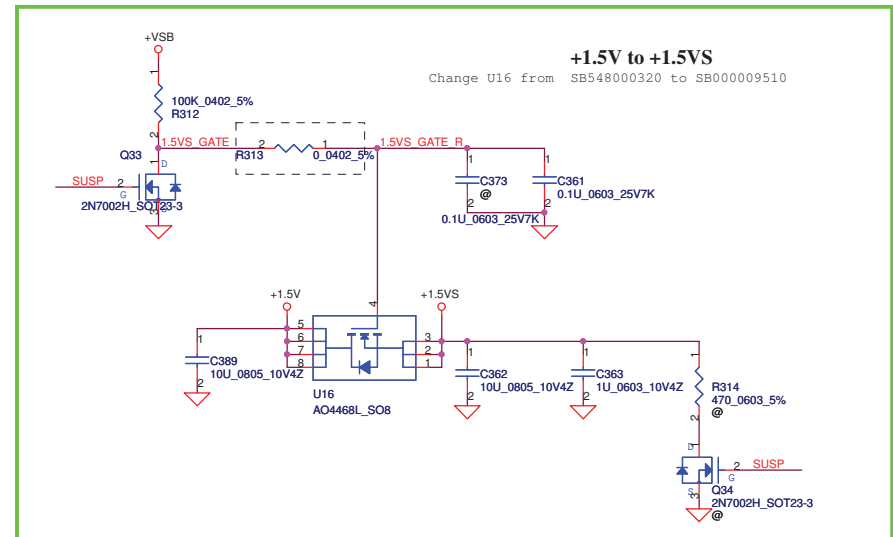
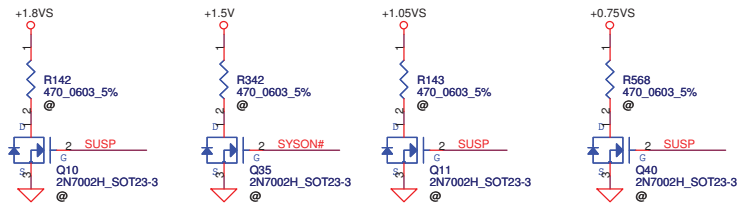
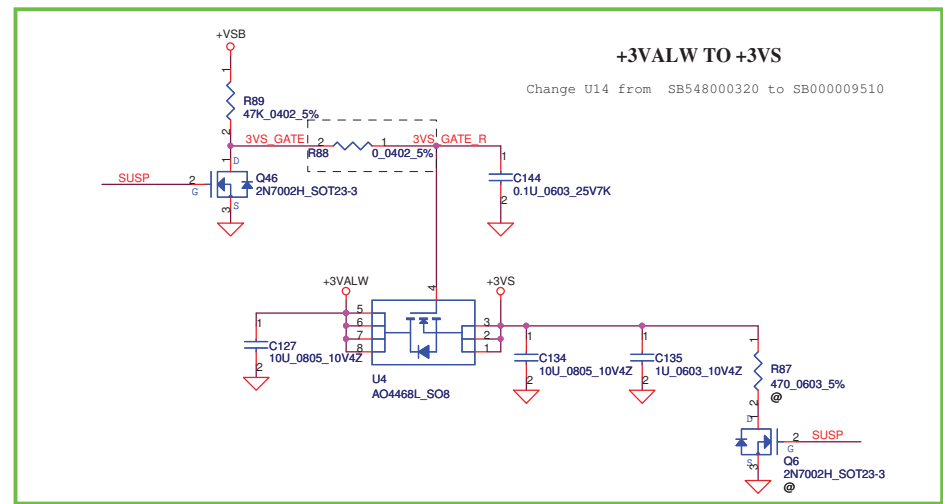
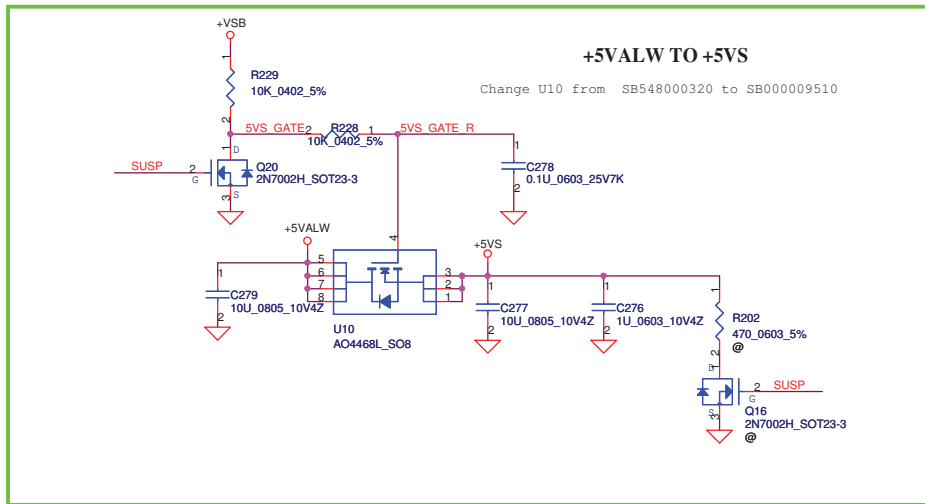
BT MODULE CONN



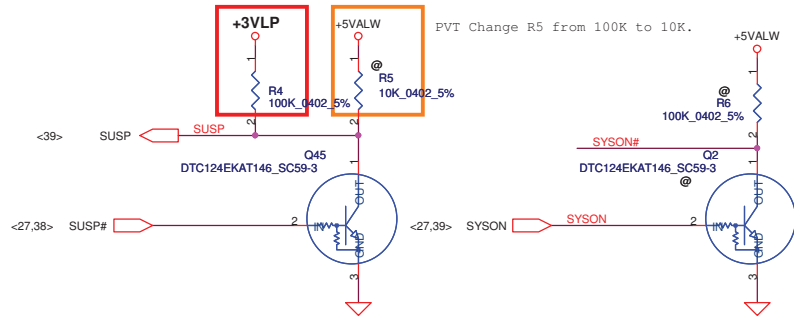
Card Reader/Audio Jack SB CONN



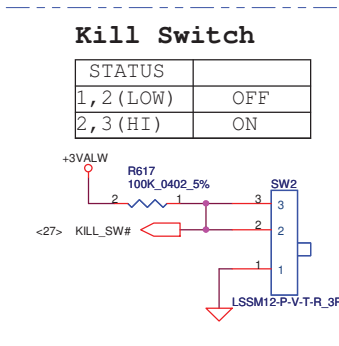
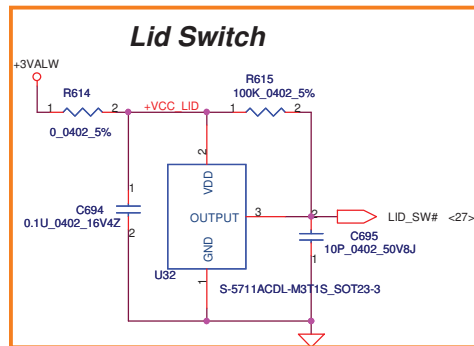
Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	Audio Jack & SW & BT Conn.
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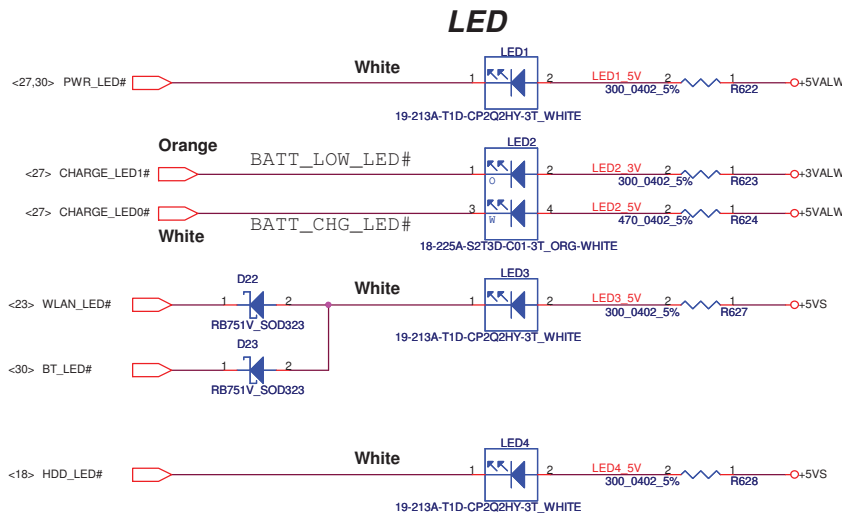
Pre MP Change SUSP pull high from +5VALW to +3VLP.



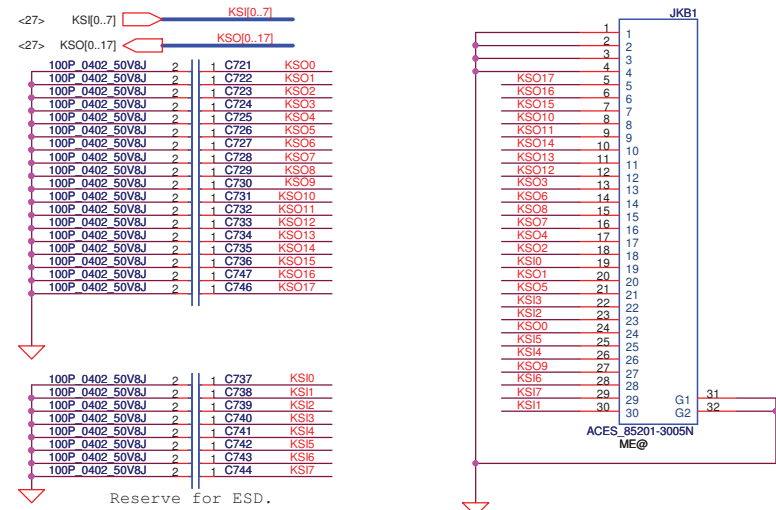
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Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	
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PVT Change U32 part number from SA032120010 to SA000031C00



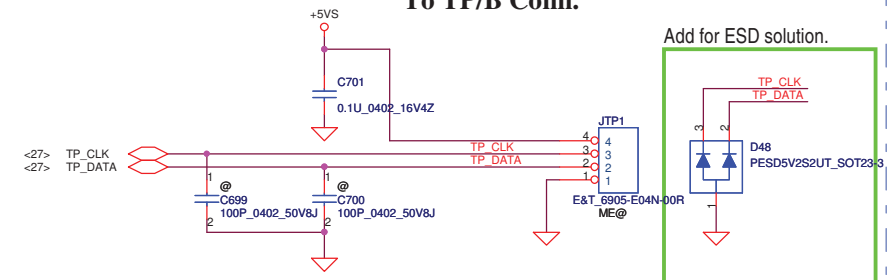
INT_KBD Conn.



check connector & pin define.

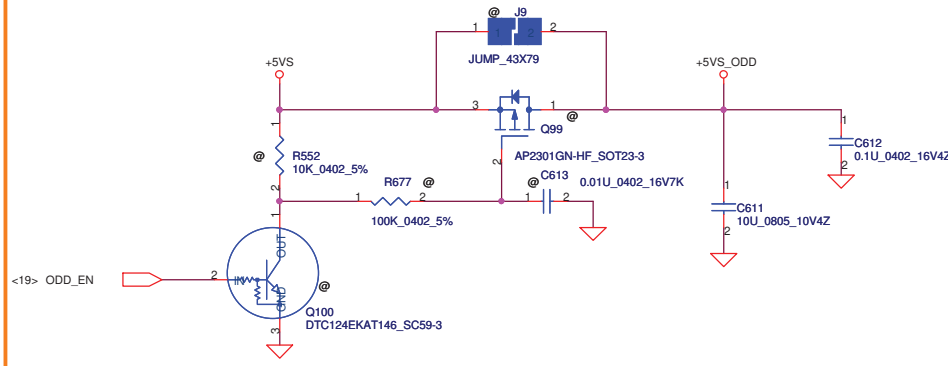
CONN PIN define need double check

To TP/B Conn.

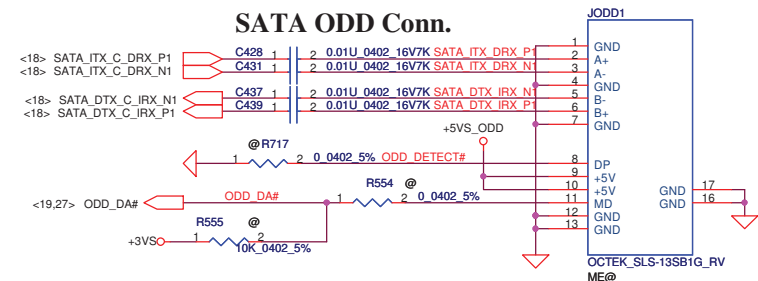


ODD Power Control

11/05 Add this function.



SATA ODD Conn.



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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
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Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title HW PIR	
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DC030006J00

VIN

4602-Q04C-09R 4P P2.5 JDCIN1

7A_24VDC_429007.WRML

APDIN1

PF1

PL1

SMB3025500YA_2P

PC122 1000P_0402_50V7K

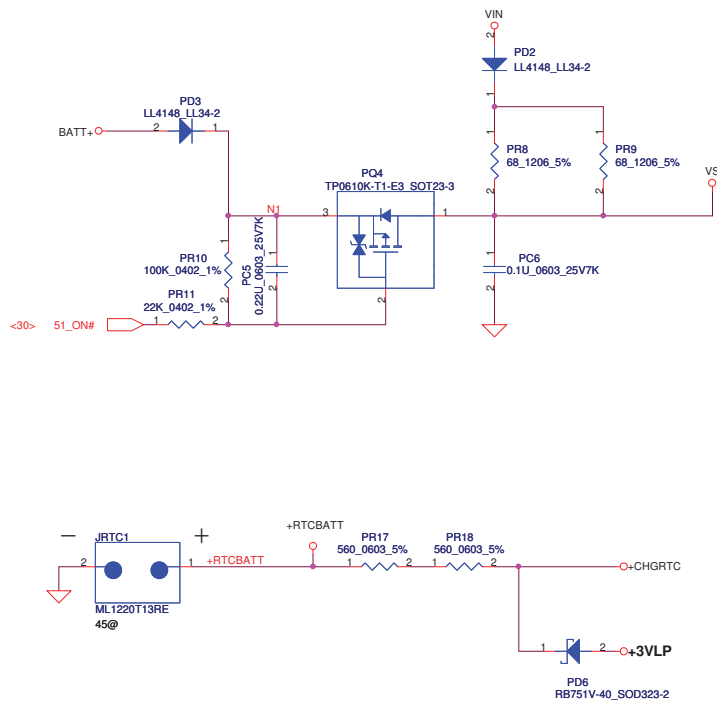
PC1 1000P_0402_50V7K

PC2 1000P_0402_50V8J

PC123 1000P_0402_50V7K

PC3 1000P_0402_50V8J

PC4 1000P_0402_50V7K



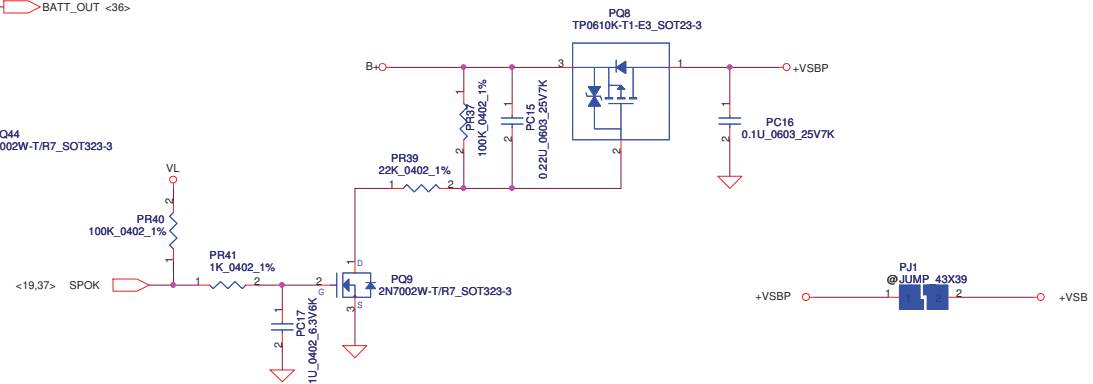
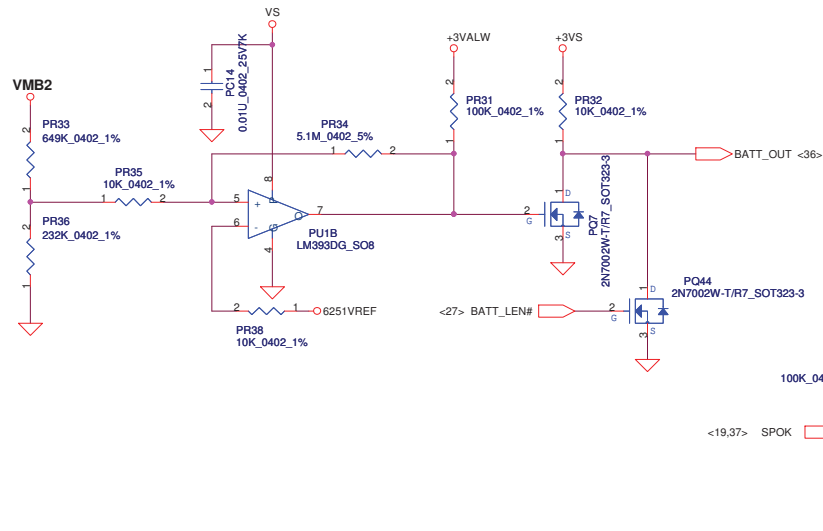
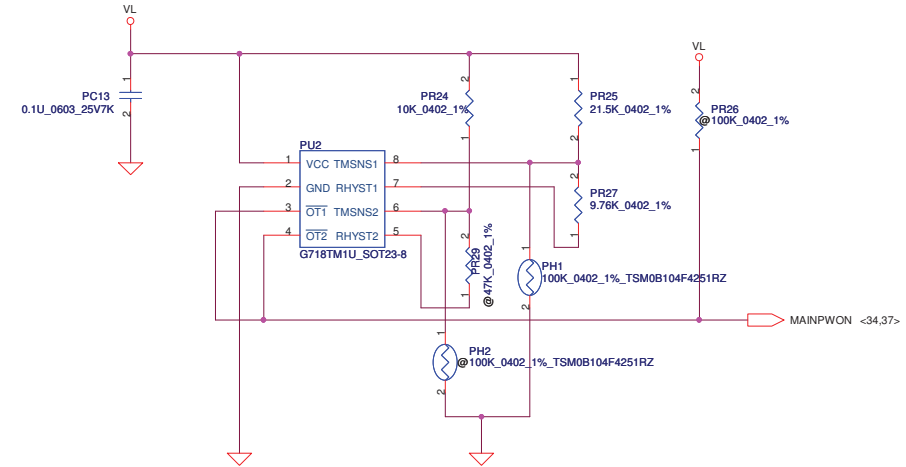
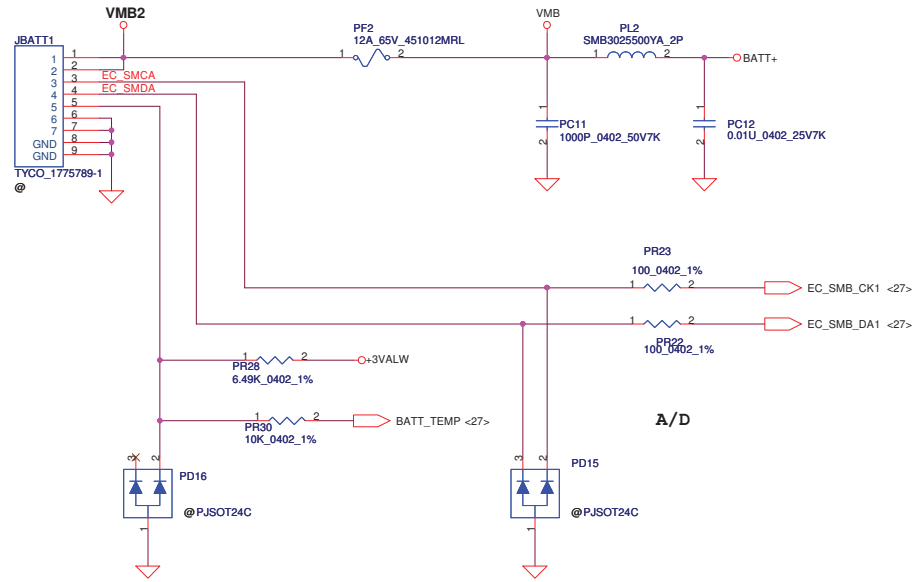
	Precharge detector		
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

	Precharge detector		
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

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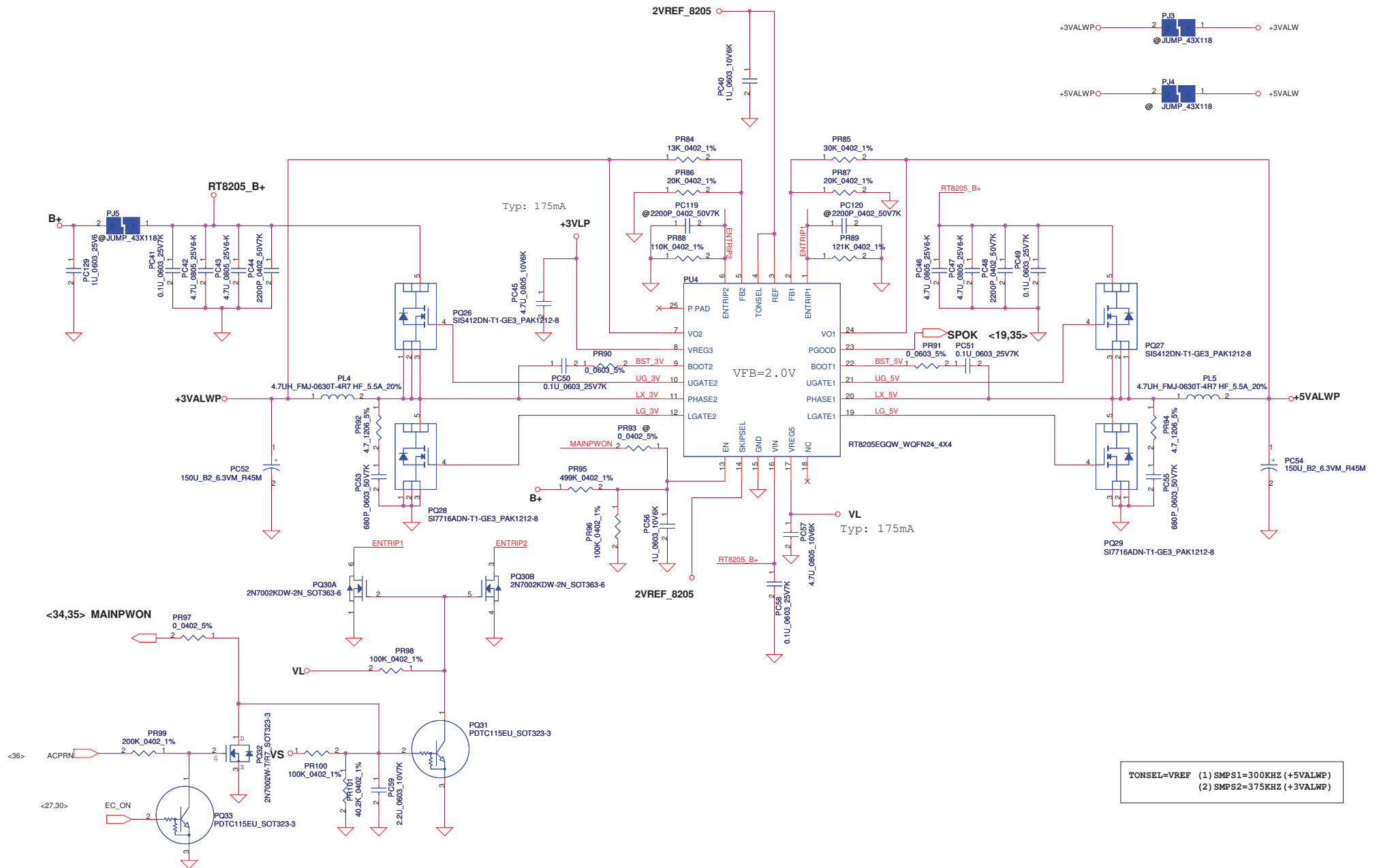
PH1 under CPU botten side :

CPU thermal protection at 92 degree C
Recovery at 56 degree C



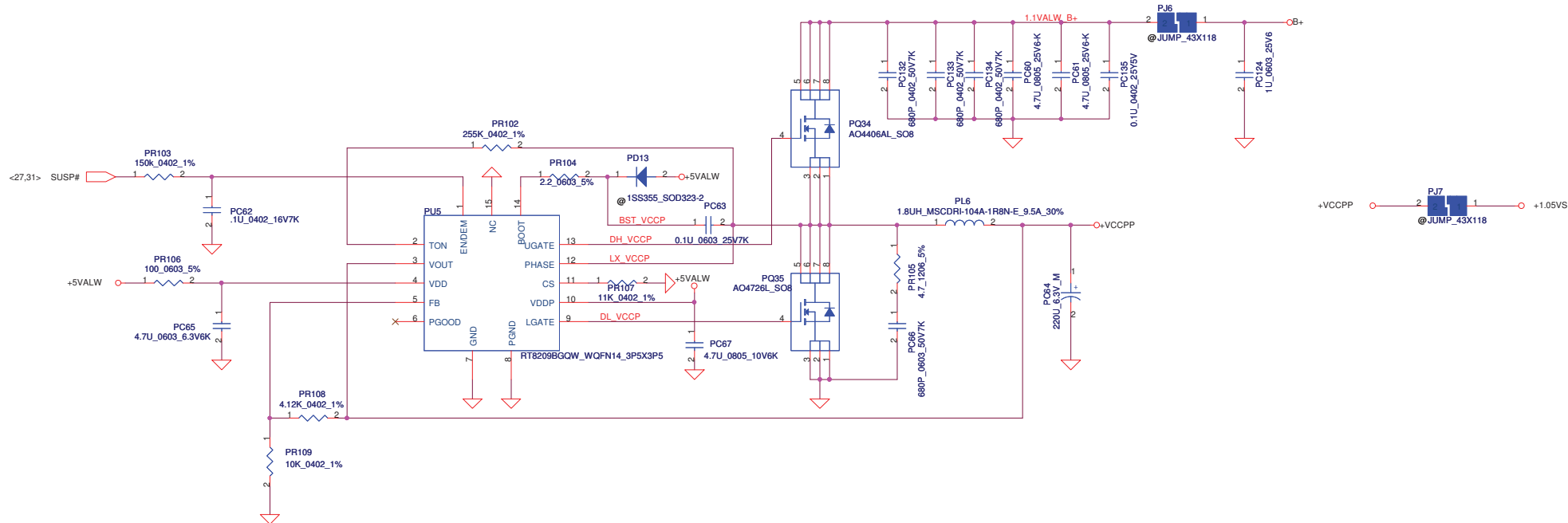
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Note:
 Use TPS51125 IC can remove RTC refernece LDO
 Use TPS51427 IC must keep RTC refernece LDO



TONSEL=VREF (1) SMP2=300KHZ (+5VALWP)
 (2) SMP2=375KHZ (+3VALWP)

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Version Change List (P. I. R. List) for Power Circuit

Page#	Title	Date	Request Owner	Issue Description	Solution Description
P35,37,39	Add capacities for EMI request	2010.11.12	EMI	EMI test fail	Add PC132,PC133,PC134,PC135,PC136,PC137
P37	Change resistance for EMI request	2010.11.12	EMI	EMI test fail	Change PR104 from 0 ohm to 2.2ohm
P35	Add one capacitor for prevent inrush current too large	2010.11.12	PWR	If there isn't add capacity, the MOS of PQ11 have damaged risk.	Add PC131 which value is 5600PF
P34	Add one transistor for improve design margin	2010.11.12	PWR	If there isn't add transistor, the design margin of PQ11 is not enough.	Add PQ44
P39	Change resistance for CPU loadline fine tuning	2010.11.12	PWR	For meet the load line of intel spec	Change PR138 from 4.3k to 4.75k
P35	Add one capacitor for improve ripple current	2010.11.12	PWR	For meet the ripple current spec of Compal	Add PC130

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2010/09/10		2010/08/19		LA7011P	
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